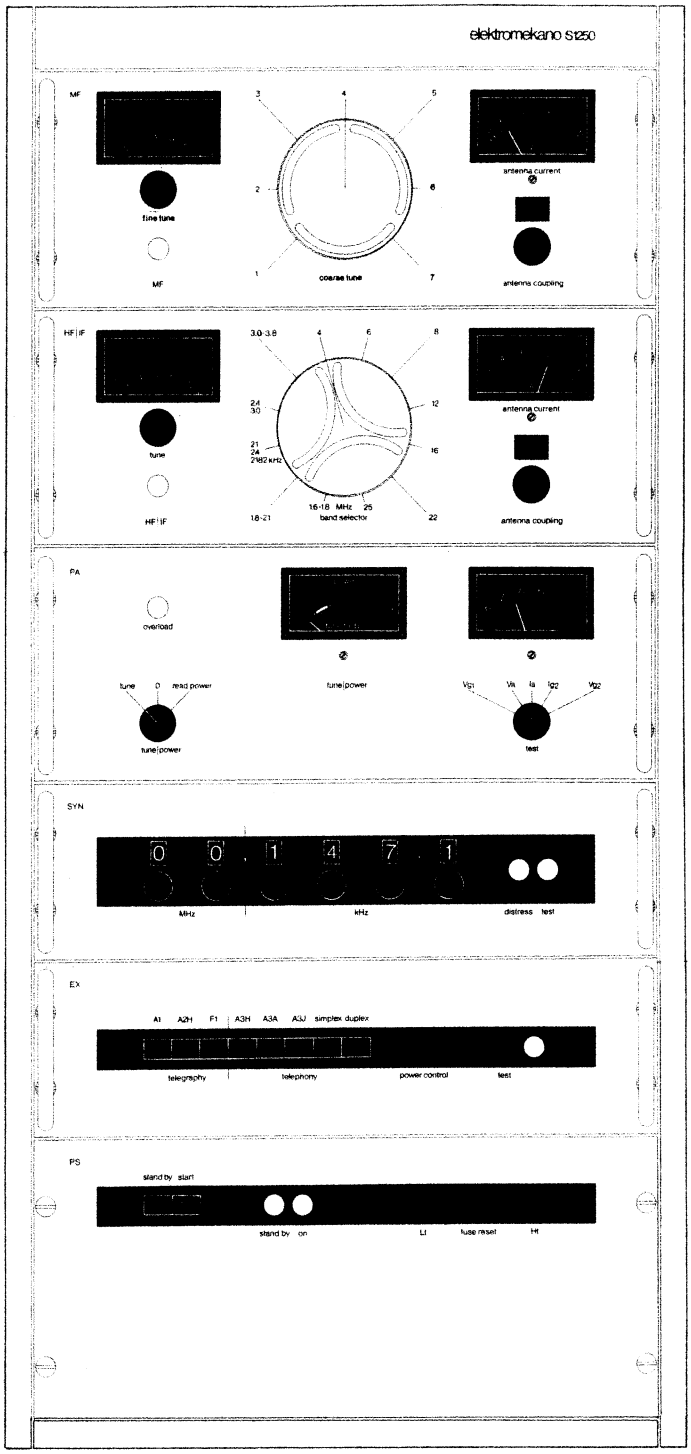
instruction manual

MAIN RADIO TELEGRAPH AND TELEPHONE TRANSMITTER

elektromekano S1250

part 1. description and parts list



1980-10

The information given in this manual at the time of publication is valid. However, the products are, as a consequence of DANSK RADIO's continuous research and development, subject to alteration without obligation of prior notice.

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SECTION 1. - TECHNICAL SPECIFICATION.

General:

This radio equipment is intended for use as a ship's main transmitter providing complete coverage of all frequencies in the maritime mobile bands for telegraphy between 405 and 535 kHz and of all frequencies in the maritime mobile bands for telegraphy and telephony between 1.6 and 27.5 MHz.

The transmitter complies with the relevant rules of the International Conference on Safety of Life at Sea (London 1960) and the Radio Regulations (Geneva 1957 and 1967), besides a number of national regulations. It also complies with the C.C.I.R. recommendation No.258-1 (Oslo 1966) in respect of S.S.B. equipment for maritime mobile use.

The transmitter consists of six panel units, the medium-frequency tuning unit, the high-frequency tuning unit, the power amplifier, the frequency synthesizer, the S.S.B. exciter and the power supply unit, which are housed in a single cabinet rack. The panel units are designed to conform to standard 19-inch rack dimensions.

Frequency Ranges:

All desired frequencies are derived from a digital type synthesizer which covers the frequency range 0-30 MHz, the frequency increment being 0.1 kHz. The frequency synthesis method is based on phase-locking the output frequency to a fixed reference frequency. The transmitting frequencies are selected by six control knobs on the front panel of the synthesizer.

In the 405-535 kHz range the output circuit of the transmitter is pre-adjusted to seven different frequencies, 410, 425, 454, 468, 480, 500 and 512 kHz, which are selected by a single control knob. The antenna circuit is fine-adjusted by a separate control knob.

In the 1.6-27.5 MHz range the output circuit of the transmitter is pre-adjusted to twelve different bands within the range, i.e. the bands 1.6-1.8, 1.8-2.1, 2.1-2.4, 2.4-3.0 and 3.0-3.8 MHz in the intermediate-frequency range, and the 4-, 6-, 8-, 12-, 16-, 22- and 25-MHz bands in the high-frequency range. These bands are selected by a single control knob while fine tuning of the circuit to the frequency in question is made by a separate control knob.

Frequency Tolerance:

short term	(15 minutes):	± 1 Hz
long term	(3 months):	± 30 Hz

Frequency Checking:

The reference oscillator circuit is so arranged that the reference frequency can easily be checked against a frequency standard, e.g. one of the 5-, 10- or 20-MHz standard frequency transmissions. An ordinary receiver may be used for detecting the signals (beat-note method).

Types of Emission:

Telegraphy: A1, A2H and F1 (externally connected tone-shift oscillator or telex equipment).
On A2H the modulation frequency is approximately 700 Hz and the carrier suppression 5 to 6 dB below p.e.p.

	Telephony: A3H, A3A and A3J. The upper sideband is transmitted.
Output Power:	405-535 kHz: 400 W p.e.p. to antenna 1605-3800 kHz: 400 W p.e.p. to antenna 4-27.5 MHz: 1200 W p.e.p. to antenna
Power Reduction:	The output power can be reduced continuously from maximum output to zero.
Antenna Impedance:	The transmitter is intended for use on antennas with the following parameters: 405-535 kHz: From 1.9 Ω in series with 750pF to 3.6 Ω in series with 300pF. 1605-3800 kHz: From 6 Ω in series with 150pF to 40 Ω in series with 250pF and 8 μH. 4-27.5 MHz: From 20 Ω to 2000 Ω (unbalanced).
Audio-Frequency Input:	Min. input voltage: 5 to 10 mV for full modulation. The input circuit is provided with attenuators for impedance matching and input level adjustment. Input for carbon microphone is standard. If required, a dynamic microphone may be used.
Audio-Frequency Band:	350-2700 Hz within 6 dB.
Speech Compression and Peak Clipping:	The A.F. amplifier includes a compressor which maintains the output power at an almost constant level, within 0.5 dB, for a microphone input level variation of 26 dB. In order to limit rapid signal peaks a clipper followed by a filter is inserted in the output circuit of the A.F. amplifier.
A.F. Distortion:	Less than 10 %.
Intermodulation Products:	In band: At least 31 dB below p.e.p. Out of band: 3rd order: At least 28 dB below p.e.p. 5th order: At least 38 dB below p.e.p. 7th order: At least 43 dB below p.e.p.
Spurious and R.F. Harmonic Suppression:	At least 45 dB below the mean power of the fundamental.
Carrier Suppression:	A3A: 16±2 dB below p.e.p. A3H: 5 to 6 dB below p.e.p. A3J: At least 40 dB below p.e.p.
Unwanted (Lower) Sideband Suppression:	At least 45 dB below p.e.p.
Hum and Noise:	At least 45 dB below p.e.p.

Unwanted Frequency Modulation:	Less than ± 10 Hz
Keying Speed:	Up to 30 bauds (approximately 40 words/min.)
Climatic Standards:	The transmitter is designed and constructed to operate in ambient temperatures from -15°C to +55°C and in relative humidity up to 95 % at +40°C.
Power Amplifier Valve:	Type 4CX1500B (8660)
Power Supply:	The transmitter is designed to operate from a 3-phase power source, 3x380V or 3x440V, 50 to 60 Hz. Mains voltage tolerance ± 10 %.
Power Consumption:	Max. 3 kVA at a power factor of 0.95.

Dimensions and Weight:	Height:	1300 mm	(incl. antenna insulator)
	Width:	530 mm	
	Depth:	600 mm	
	Weight:	approx. 165 kg	

2.1. Mechanical Description.

The transmitter consists mainly of six units which are housed in a standard 19-inch cabinet rack. The arrangement of the units in the cabinet rack is illustrated below.

Medium-Frequency Antenna Matching Network
Reference Designation: A6

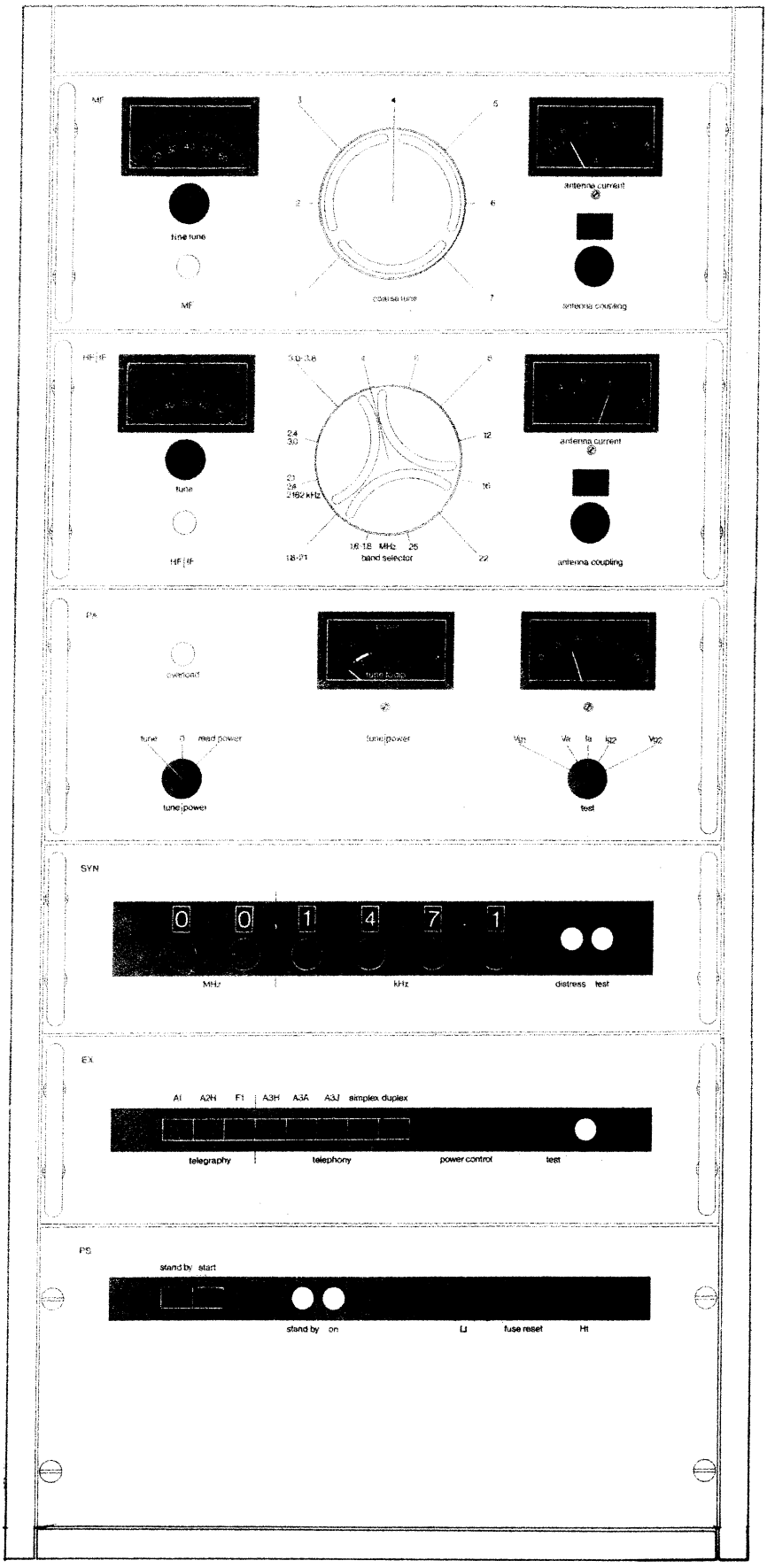
High-Frequency and Intermediate-Frequency Antenna Matching Network
Reference Designation: A5

Power Amplifier Unit.
Reference Designation: A4
Sub-Assemblies:
A4A1 and A4A2

Synthesizer Unit.
Reference Designation: A3
Sub-Assemblies:
A3A1, A3A2, A3A3, etc.

S.S.B. Exciter Unit.
Reference Designation: A2
Sub-Assemblies:
A2A1, A2A2, A2A3, etc.

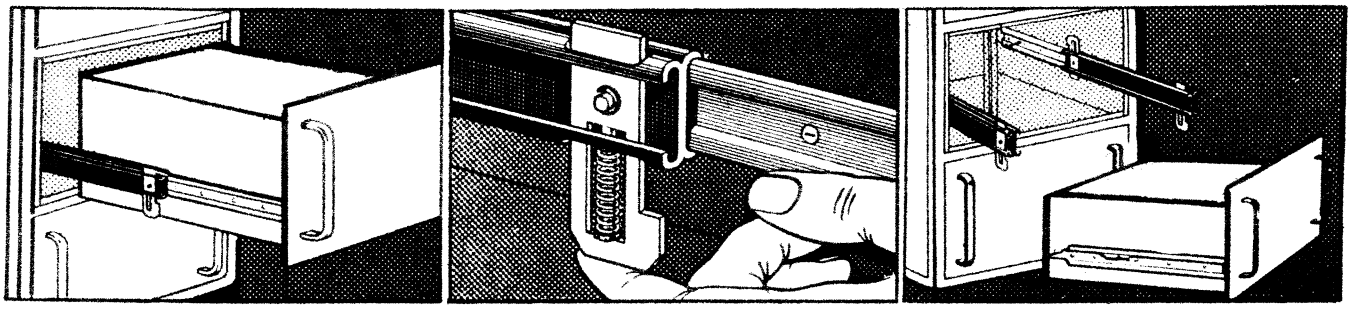
Power Supply Unit.
Reference Designation: A1
Sub-Assemblies:
A1A1 and A1A2



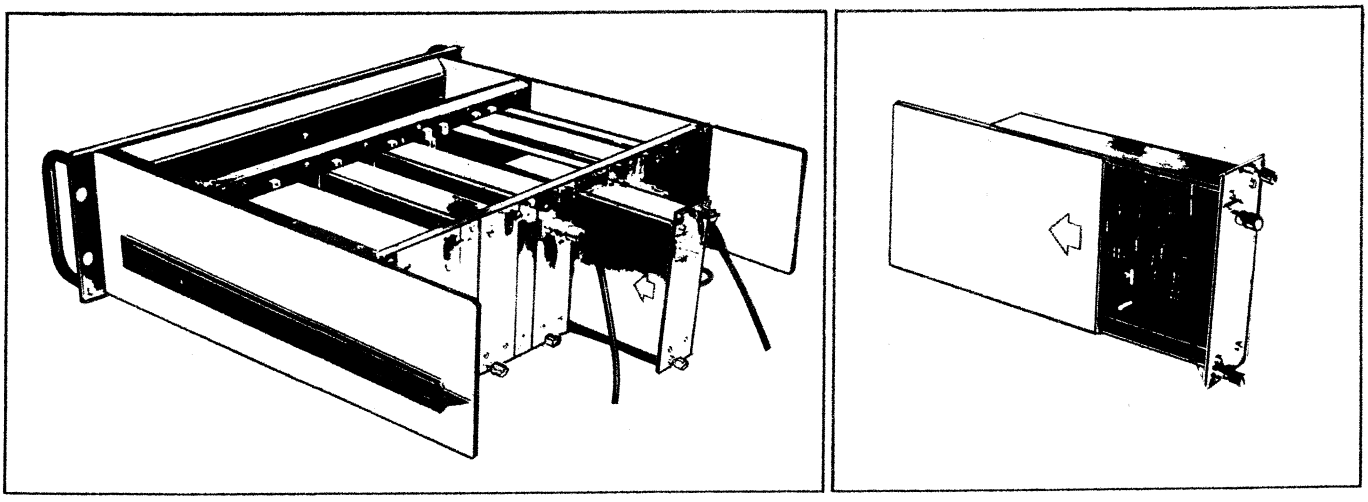
Cabinet Rack.

The power supply unit is mounted on a strong chassis which rests on the bottom framework of the cabinet rack and is fastened by two holders at the rear and two screws at the front, one at each side. The front panel is fastened to the cabinet rack by four screws. The power supply unit can be pulled out from the cabinet rack when its front panel is removed and the two screws at the front of the chassis are unscrewed. When the multi-conductor plug at the rear of the chassis is taken out of its socket the power supply unit can be completely removed from the cabinet rack.

The other units are designed as drawers (panel-and-chassis assemblies) mounted on telescopic slides. The front panels are fastened to the cabinet rack by means of captive panel-mounting screws. The telescopic slides are fitted with trigger latches which automatically and securely lock the unit in the withdrawn position, when fully extended. The projecting latches are pressed to release the lock so that the drawer can be closed or completely removed from the cabinet rack as shown below. Before removing a drawer from the cabinet all plugs on cables for connecting the unit to the cabinet wiring should be taken out of their sockets at the rear of the chassis.

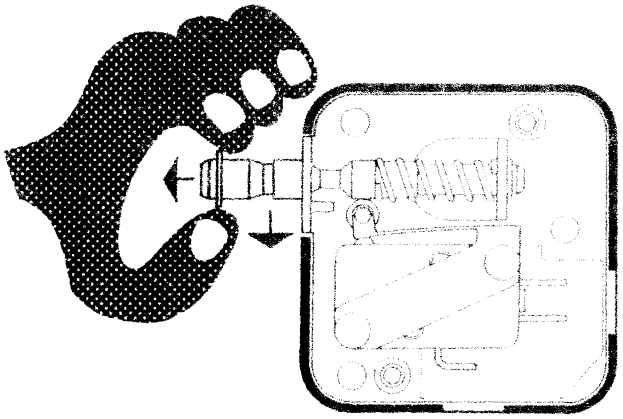


The rear of the chassis of the S.S.B. exciter unit and the synthesizer unit is formed as a miniature rack into which plug-in modules (sub-assemblies) of various widths are inserted. The electrical connections between the modules and other parts of the transmitter are made by means of printed-circuit card connectors, and for some of the modules coaxial-cable connectors or multi-conductor connectors are provided on the module panels. The modules are fastened to the frame of the drawer by means of captive panel-mounting screws. Slide-out side covers are provided on the modules for easy access to the circuit cards. See illustrations below.

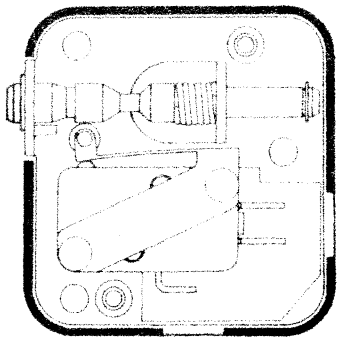


The six units are electrically connected with the wiring of the cabinet rack by means of flexible cables with plugs and sockets at the chassis end and terminal blocks at the cabinet

end. Some of the units are also equipped with plug-in contacts (knife and spring clip contacts). Interlock switches are provided to prevent operating personnel from accidentally coming in contact with high voltage when units (drawers) are withdrawn. These interlock switches (door switches) are located inside the cabinet rack to the left, one for each unit. In order to be able to carry out 'live' inspection the maintenance engineer may set an interlock switch in the 'locked-on' position, see illustrations below.



Pull plunger down and out for 'locked-on' position during maintenance.



Full interlock protection is automatically restored on the first closure of the panel.

It is emphasized, however, that since the mains voltage is also dangerous to life, the main switch outside the transmitter must always be opened if some work is to be done inside the transmitter.

An antenna lead-through insulator with a terminal for connecting the antenna is provided on top of the cabinet rack and a terminal for ground connection is located on the back of the cabinet rack near the top. A terminal block for connecting the external wiring cables to the transmitter is located inside the cabinet rack on the rear plate near an entering slot through which the cables are passed. Inlet and exhaust vents for a blower in the power amplifier unit are provided in the rear plate of the cabinet rack. The inlet vent is equipped with an air filter. The mounting dimensions of the transmitter are shown on the outline dimensional drawing which is located in the drawing section at the rear of this manual.

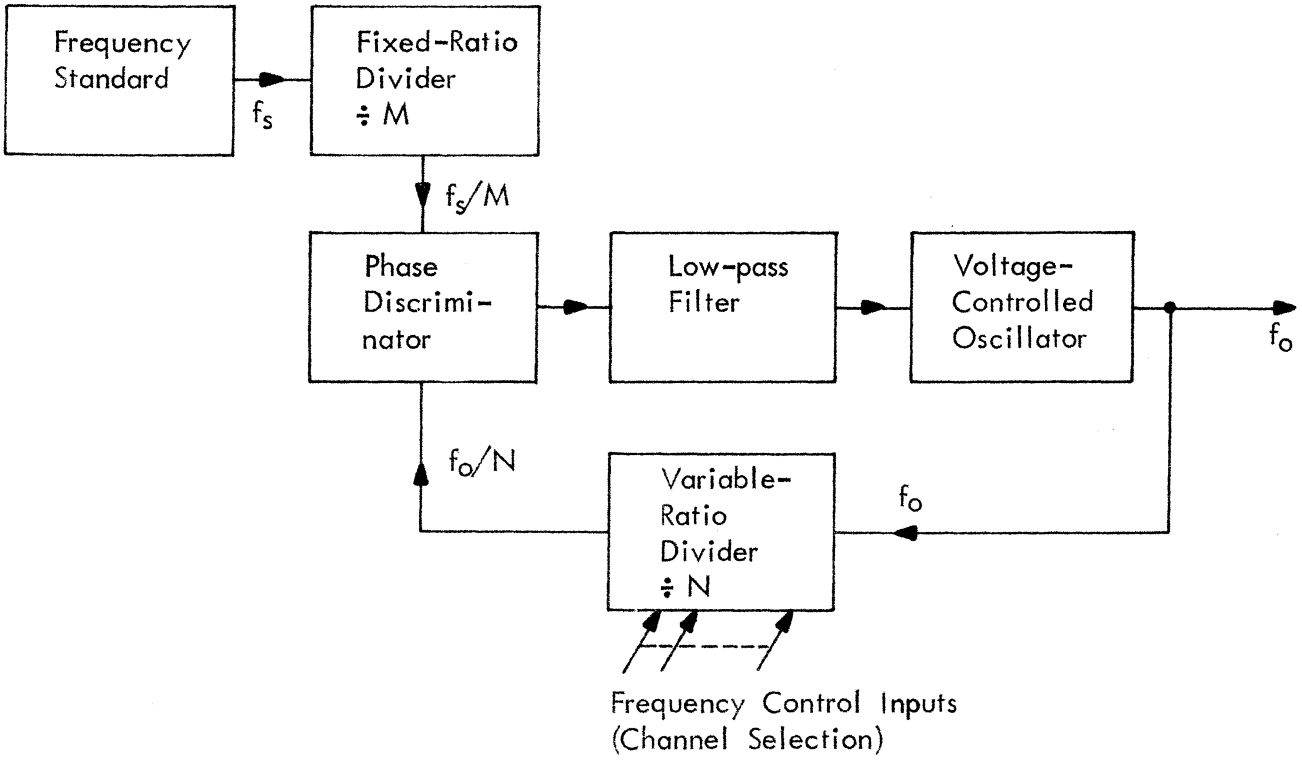
2.2. Electrical Description.

2.2.1. Block Diagram.

A complete block diagram of the transmitter is located in the diagram section at the rear of this manual. This block diagram shows the overall relationship between all major circuits in the transmitter. The identification number on each block is the same as that used in the text. The blocks are divided into groups corresponding to the assemblies and subassemblies of the transmitter for which complete circuit diagrams are also provided at the rear of this manual. The reference designations of the assemblies and subassemblies corresponding to the groups are shown in the block diagram. Only the basic interconnections are shown. The power-supply units are omitted.

2.2.1.1. Frequency Synthesizer. Reference Designation A3.

The principle of operation of a single-loop synthesizer is shown below in a simplified block diagram. All the frequencies necessary for the single-sideband signal processing are derived from a single frequency standard which consists of a very stable crystal oscillator. The signal of frequency f_S produced by this oscillator is applied to a phase discriminator (comparator) via a frequency divider with a fixed division ratio M. The resulting frequency f_S/M, the reference frequency, is equal to the channel spacing. A tunable voltage-controlled oscillator can cover the desired range or can be switched in steps to cover various bands in the range. Coarse prepositioning information is supplied when the channel is selected. A digital divider,



whose division ratio N is variable, divides the frequency f_O of the voltage-controlled oscillator by the proper ratio to provide an output at approximately the reference frequency. This output signal is compared with the reference frequency f_S/M in the phase discriminator. Any difference in phase between the two frequencies f_S/M and f_O/N will result in a d.c. error voltage which is fed back through a low-pass filter to the voltage-controlled oscillator. The low-pass filter serves to filter components of the input frequencies and their harmonics from the output in order to prevent frequency modulation of the voltage-controlled oscillator. When the output frequency of the voltage-controlled oscillator is corrected to provide the

proper input frequency to the phase discriminator, it phase-locks the loop "(voltage-controlled oscillator)-(divider ÷ N)-(phase discriminator)-(low-pass filter)-(voltage-controlled oscillator)" to the reference input and, since $f_o/N = f_s/M$, the output frequency of the voltage-controlled oscillator can be expressed as

$$f_o = N\,(f_s/M).$$

From this equation it will be seen that any desired multiple of the reference frequency f_s/M can be produced by selecting the necessary division ratio N in the variable-ratio divider. This is done automatically by the channel selection switches. The stability of the produced frequencies will be equal to that of the frequency standard.

One of the main advantages of this method of synthesis is its freedom from spurious signals in the output, and in this respect it is superior to the conventional method in which the signal frequency is obtained by successive mixing and filtering. However, it may be difficult to obtain sufficient filtering of the components of the reference frequency in the system described above. If the time constant of the filter is long the short-term stability of the voltage-controlled oscillator must be high, and if the time constant of the filter is short the rejection of the components of the reference frequency will not be sufficiently effective. Therefore a compromise between the two points of view must be made.

To enable the synthesizer to provide complete coverage of all frequencies used in the maritime mobile service, the reference frequency should be as low as 100 Hz. However, by introducing an extra phase-locked loop in the actual synthesizer, it has been possible to use a reference frequency of 500 Hz whereby the above mentioned problem has been solved. Three signal frequencies are necessary for signal processing in this system of synthesis, i.e. a fixed frequency of 1.5 MHz, a variable frequency in the range 33.4991 MHz to 33.5000 MHz and a variable frequency in the range 35 MHz to 65 MHz. The fixed frequency of 1.5 MHz is derived from a 7.5-MHz crystal-controlled oscillator (frequency standard) the output frequency of which is divided by 5. The frequency in the range 33.4991 MHz to 33.5000 MHz is derived from a voltage-controlled crystal oscillator and frequency multiplier circuit with a loop feedback system by means of which the output frequency can be phase-locked in steps of 100 Hz. The use of a crystal-controlled oscillator in this circuit makes it possible to achieve the desired very high short-term frequency stability. The frequency in the range 35 MHz to 65 MHz is derived from a voltage-controlled oscillator circuit with a loop feedback system by means of which the output frequency can be phase-locked in steps of 1 kHz.

The standard-frequency signal of 7.5 MHz is produced by the crystal-controlled oscillator shown as block 1 in the complete block diagram of the transmitter. The output frequency of this oscillator is divided by 5 in block 2 and the 1.5-MHz output is applied to block 3 as well as to block 4. Block 3 contains a 1.5-MHz selective amplifier the output of which is applied to the S.S.B. exciter. Block 4 contains a frequency divider which divides the 1.5-MHz signal by 3. The 500-kHz output from this divider is applied to block 5 as well as to block 6. Block 5 contains a differentiating circuit which produces appropriate multiples of the 500-kHz signal for checking the frequency standard against one of the 5-, 10- or 20-MHz standard-frequency transmissions, e.g. the WWV transmissions. The 500-kHz signal from block 4 is also fed to block 6 which contains a frequency divider with a division ratio of 1000, and from this divider the required output frequency of 500 Hz, the reference frequency, is obtained. The 7.5-MHz signal from the frequency standard, block 1, is also applied to block 7 which contains a frequency multiplier. In block 7 the 7.5-MHz signal is multiplied by 4 to produce an output signal of 30 MHz for signal processing in the 33.4991-33.5000 MHz loop system. Appropriate filtering of the 30-MHz output signal from the multiplier is provided by a band-pass filter contained in block 8.

33.4991-33.5000 MHz loop system:- A voltage-controlled crystal oscillator contained in block 9 is designed to produce a frequency which, by means of the loop feedback system, can be phase-locked in steps of 100 Hz within the range 3.4991 MHz to 3.5000 MHz. The output frequency from this oscillator is multiplied by 5 in a frequency multiplier contained in block

10. Appropriate filtering of the output signal from the multiplier is provided by a band-pass filter contained in block 11. The frequency of the output signal from the filter will lie within the range 17.4955 MHz to 17.5000 MHz, the actual frequency being dependent on the oscillator control voltage. The output signal from the filter is applied to a variable-ratio frequency divider which is contained in the blocks 12 and 13. Division ratios of 34991, 34992, etc. to 35000 can be selected by a 10-position switch in the decade contained in block 14, the 1st decade. The output signal from the variable-ratio frequency divider is fed to a phase discriminator contained in block 14 where it is compared with the reference frequency of 500 Hz. The output from the phase discriminator is fed to the control terminal of the voltage-controlled crystal oscillator via a low-pass filter contained in block 15, thus completing the loop. With this loop system the voltage-controlled oscillator can be phase-locked in steps of 100 Hz within the said range, the actual frequency being determined by the setting of the decade switch. The output signal from the voltage-controlled crystal oscillator, block 9, is fed to a mixer contained in block 16 together with the 30-MHz signal from block 8 to produce a signal which has a frequency equal to the sum of the two input frequencies, i.e. the frequency of the output signal will lie within the range 33.4991 MHz to 33.5000 MHz, the actual frequency being determined by the setting of the decade switch in block 14. A band-pass filter contained in block 17 rejects the undesired difference frequency signal from the mixer and passes the above mentioned signal, the desired signal, on to an amplifier contained in block 18.

The output signal from the amplifier contained in block 18 is fed to the S.S.B. exciter where it is mixed with the 1.5-MHz signal to produce a signal which will lie within the range 34.9991 MHz to 35.0000 MHz. This signal is finally mixed with a signal in the range 35 MHz to 65 MHz to produce the desired transmitting frequency in the range 0 to 30 MHz. It should be noted that the above mentioned frequency 34.9991 MHz, which is the lowest frequency in the range, corresponds to the highest digit, 9, in the 1st decade, and that the frequency 35.0000 MHz, which is the highest frequency in the range, corresponds to the lowest digit, 0, in the 1st decade. In this respect the coding of the 1st decade differs from that of the other decades as described later in this manual.

35-65 MHz loop system:- A voltage-controlled oscillator contained in block 19 is designed to produce a frequency which, by means of the loop feedback system, can be phase-locked in steps of 1 kHz within the range 35 MHz to 65 MHz. The output signal from this oscillator is applied to a dual-channel amplifier contained in block 20. In order to prevent transmission during frequency shift, this amplifier is so arranged that its output channel is blocked when the loop is not phase-locked. The oscillator output signal is fed to a prescaler contained in block 21 through one of the channels of the amplifier. In the prescaler the frequency of the signal is divided by 2 and the resulting signal, the frequency of which will lie within the range 17.5 MHz to 32.5 MHz, is applied to a 5-decade digitally coded frequency divider system contained in the blocks 22 to 26. This frequency divider can be preset to divide the frequency by any integer between 35000 and 64999 by means of 5 binary coded switches controlling the 5 decades. The output signal from the 5-decade frequency divider is fed to a phase discriminator contained in block 27 where it is compared with the reference frequency of 500 Hz. The output from the phase discriminator is fed to the control terminal of the voltage-controlled oscillator via a low-pass filter contained in block 28, thus completing the loop. With this loop system the voltage-controlled oscillator can be phase-locked in steps of 1 kHz within the range 35.000 MHz to 64.999 MHz, the actual frequency being determined by the setting of the 5 decade switches.

Since the frequency range of the voltage-controlled oscillator is relatively wide in comparison with the capture range of the loop, special means for appropriate coarse tuning of the oscillator circuit must be provided. In order to fulfil this requirement an 8-bit binary up-down counter contained in block 29 and a digital-to-analogue converter contained in block 30 are introduced in the circuit. The phase discriminator is designed to produce clock pulses when the loop is not phase-locked. These clock pulses are applied to the 8-bit binary up-

down counter. If the oscillator frequency is too low the counter counts down, and if the oscillator frequency is too high the counter counts up. The first 6 bits control the digital-to-analogue converter which produces the control signal for coarse tuning of the oscillator. This control signal is applied to the input of the low-pass filter contained in block 28 where it is added to the error signal from the phase discriminator. The last two bits of the binary up-down counter are decoded to control four switching diodes by means of which the proper tap on the oscillator inductor for coarse-tuning the voltage-controlled oscillator to the required frequency is selected. Thus, if the oscillator frequency is too low or too high, the counter will count down or up, respectively, until the oscillator frequency is brought inside the capture range of the loop, after which phase locking is established. It should be noted that the tuning procedure is completely controlled by electronic means whereby extremely high reliability is ensured.

The exact operating range of the transmitter obtained by means of the synthesizer and mixers described above is 0 to 29.9999 MHz in 100-Hz steps.

2.2.1.2. Single-Sideband Exciter. Reference Designation A2.

The functions of the s.s.b. exciter are controlled by means of an electronic function control circuit which is contained in block 41 in the complete block diagram of the transmitter. Input informations on the following types of emission are provided by a type-of-emission selector contained in block 42: A1, A2H, F1, A3H, A3A and A3J. This selector also provides input informations on simplex and duplex operation. Input informations to the function control circuit are also provided by the following parts of the transmitter equipment: telegraph key contacts, press-to-talk switch contacts, "tune" switch contacts, "test" switch contacts, interlocking switch contacts and appropriate switch contacts in the synthesizer for the frequencies 500 kHz and 2182 kHz. The circuits which are controlled by the function control circuit are described in the following.

The audio-frequency input circuit of the exciter can be connected to either a microphone, a frequency-shift keying (f.s.k.) signal source or an 700-Hz oscillator by means of an input selector contained in block 43. This selector is controlled by the function control circuit mentioned above. The 700-Hz oscillator is contained in block 44. The switching on and off of this oscillator is also controlled by the function control circuit so that the oscillator is on only when its output is switched to the a.f. input of the exciter. If any of the types of emission A3H, A3A and A3J are selected by the selector in block 42, the function control circuit in block 41 causes the selector in block 43 to switch the microphone to the a.f. input circuit of the exciter. If the type of emission F1 is selected, the a.f. input circuit of the exciter is switched to the terminals for the f.s.k. signal. If the type of emission A2H is selected, the 700-Hz oscillator is switched on and its output is connected to the a.f. input circuit of the exciter. When the synthesizer is set on 500 kHz the s.s.b. exciter is unconditionally adjusted for A2H operation by means of the function control circuit. Similarly, when the synthesizer is set on 2182 kHz the s.s.b. exciter is automatically adjusted for A3H operation with the microphone connected to the a.f. input circuit, but if the tune switch is turned on the 700-Hz oscillator is switched on and connected to the a.f. input circuit. When the tune switch is turned on or the test push-button switch is pressed, the s.s.b. exciter is unconditionally adjusted for operation with the 700-Hz oscillator switched on and connected to the a.f. input circuit, and keying of the exciter takes place as long as the switch in question is operated.

The a.f. input signal to the exciter is fed to a compressor contained in the blocks 45, 46 and 47. The compressor consists of a voltage-controlled attenuator, block 45, followed by an amplifier, block 46, to the output of which a rectifier, block 47, is connected. The rectified output signal is fed to the voltage-controlled attenuator so that the gain of the amplifier is automatically controlled. By this arrangement the output signal level of the amplifier is maintained almost constant, within 1.5 dB, for an input signal level variation of 20 dB.

Minimum input for full modulation 10 mV. The compressor output signal is applied to an amplifier contained in block 48. In order to limit rapid signal peaks a clipper, contained in block 49, is inserted in the output circuit of this amplifier. The clipper is followed by a low-pass filter, block 50, from the output of which the a.f. signal is applied to the output amplifier contained in block 51.

A sidetone oscillator contained in block 52 is switched on by the function control circuit when the type-of-emission selector is set in the positions for A1 and A2H operation. The 700-Hz output signal from the sidetone oscillator is fed to the external circuit, e.g. the a.f. input circuit of a receiver associated with the transmitter, through an electronic keying circuit contained in block 53. This keying circuit is controlled by the function control circuit in such a way that the sidetone signal is applied to the external circuit only when the telegraph key is closed.

The a.f. output signal from the amplifier contained in block 51 is applied to a balanced modulator, block 54, in which it modulates a 1.5-MHz carrier signal to produce a double-sideband signal with suppressed carrier. The modulator is followed by a crystal filter, block 56, which selects the lower sideband of the output signal from the modulator and provides further suppression of the carrier. The 1.5-MHz carrier signal, which is obtained from the synthesizer, is applied to the modulator through a carrier distribution circuit contained in block 55. The carrier distribution circuit, which is controlled by the function control circuit, provides means for reinsertion of the carrier at the input of the mixer contained in block 57 along with the l.s.b. signal from the crystal filter. In cases where carrier reinsertion is required, the function control circuit automatically sets the reinserted carrier to the desired level for the type of emission selected by the type-of-emission selector.

A variable-frequency carrier signal of 33.4991-33.5000 MHz, which is obtained from the synthesizer, is applied to the mixer, block 57, through a variable-gain amplifier, block 58. The gain of this amplifier is controlled by a knob on the front panel and by a pulse shaper contained in block 59. The pulse shaper is controlled by the function control circuit and the keying system of the transmitter. When the keying contacts, i.e. the keying contacts of the telegraph key, the press-to-talk switch, the tune switch, the test switch and the keying contacts for F1 operation and duplex operation, are open, the pulse shaper reduces the amplification of the variable-gain amplifier to zero so that no signal appears at the output of the mixer contained in block 57. When the type-of-emission selector is set for A1 or A2H operation the telegraph key is switched into circuit whereas when it is set for A3H, A3A or A3J operation the press-to-talk switch on the microphone or handset is switched into circuit. In cases where F1 operation or duplex operation is selected the s.s.b. exciter is keyed continuously. Keying of the exciter also takes place when the tune switch or the test switch is operated. When the synthesizer is adjusted for operation on 500 kHz the telegraph key is unconditionally connected into circuit. The panel-operated gain control functions as a power control.

When the s.s.b. exciter is keyed the carrier signal from the output of the variable-gain amplifier is applied to the mixer contained in block 57 together with the l.s.b. signal from the output of the crystal filter, which signal may also include a reinserted 1.5-MHz signal, to produce a new l.s.b. signal with a carrier frequency equal to 1.5 MHz plus the actual frequency of the signal from the variable-gain amplifier. A band-pass filter contained in block 60 rejects the undesired difference frequency signal from the mixer and passes the desired l.s.b. signal mentioned above on to an amplifier contained in block 61. The carrier frequency of this l.s.b. signal will lie within the range 34.9991 MHz to 35.0000 MHz, the actual frequency being determined by the setting of the 1st decade switch in the synthesizer. In order to remove out-of-band noise a crystal filter contained in block 62 is provided in the output of the amplifier, block 61. The output signal from this crystal filter is applied to a mixer contained in block 63. A variable-frequency signal of 35-65 MHz, which is obtained from the synthesizer, is fed to this mixer through an amplifier contained in block 64. When

the s.s.b. exciter is keyed, the l.s.b. signal from the crystal filter is mixed with the above mentioned signal to produce an upper-sideband signal with a carrier frequency equal to the difference between the frequency of the signal from the synthesizer and the carrier frequency of the l.s.b. input signal to the mixer. A low-pass filter contained in block 65 rejects the undesired sum frequency signal from the mixer and passes the desired u.s.b. signal on to an amplifier contained in block 66. The carrier frequency of the u.s.b. signal will lie within the range 0 to 29.9999 MHz, the actual frequency being determined by the setting of the decade switches in the synthesizer.

The carrier frequency of the above mentioned u.s.b. signal is equal to the transmitting carrier frequency. In the case of A1 operation the transmitting frequency is equal to the carrier frequency. The output signal from the amplifier, block 66, is fed to a three-stage wide-band amplifier, block 68, through a low-pass filter, block 67. The amplifier, block 68, is followed by a two-stage wide-band amplifier, block 69, the output signal of which is fed to a driver preceding the power amplifier of the transmitter. The two-stage wide-band amplifier provides an output power of approximately 1 watt p.e.p. into a load of 50 Ω.

2.2.1.3. Power Amplifier and Tuning Circuits. Reference Designations A4, A5 and A6.

The output signal from the s.s.b. exciter is applied to a wide-band amplifier contained in block 80. This amplifier drives a power amplifier contained in block 81. In the frequency bands for maritime mobile service between 1.6 MHz and 27.5 MHz the power amplifier is tuned by means of an antenna matching network contained in block 90, while in the range 405 kHz to 535 kHz it is tuned by means of an antenna matching network contained in block 95. Changing between the two antenna matching networks is performed by means of a relay which is controlled by the synthesizer decade switches in such a way that the network corresponding to the frequency setting is automatically selected. Similarly, an antenna relay located in the cabinet rack automatically switches the antenna to the matching network in question. An amplitude discriminator contained in block 82 and a meter contained in block 83 provide means for adjusting the power amplifier for correct tuning and proper loading. The switches in the tuning circuits mentioned above are combined with interlocking switches which are connected to the input of the function control circuit. When these interlocking switches are closed the function control circuit causes the supply voltage for the wide-band amplifiers to be switched off. By this means the signal voltage is removed from the switches in the tuning circuit while switching over from one position to another.

2.2.2. Cabinet Rack Wiring.

The complete wiring diagram of the cabinet rack is located in the diagram section at the rear of this manual together with the circuit diagrams of the panel-and-chassis assemblies and subassemblies. A terminal board, TB1, for connecting the external wiring cables to the transmitter is located inside the cabinet on the rear plate above an entering hole through which the cables are passed. Radio-frequency filters are provided at all terminals for the external wiring cables. An antenna lead-through insulator with a terminal for connecting the antenna is provided on top of the cabinet rack and terminals for ground connection are located on the back of the cabinet rack near the top.

The six panel-and-chassis assemblies contained in the cabinet rack are electrically connected with the wiring of the cabinet rack by means of flexible cables with plugs and sockets at the chassis end and terminal strips at the cabinet end. Some assemblies are also equipped with plug-in contacts (knife and spring-clip contacts). The reference designations for the mating connectors (plugs, sockets or plug-in contacts) are added in parentheses (brackets) adjacent to the connectors shown. Cable assemblies for interconnection of two panel-and-chassis assemblies are designated by the letter W, the designation method used for the cable connectors being similar to that mentioned above. Interlock switches are provided to prevent operating personnel from accidentally coming in contact with high voltage when panel-and-chassis assemblies are withdrawn.

The antenna is automatically switched to the antenna matching network in use by means of a relay unit containing two relays, K2 and K3, located on the rear plate of the cabinet rack near the top. These relays are fed from a 24-volt d.c. supply, located in the main power-supply assembly, and controlled by the decade switches on the frequency synthesizer front panel. Four silicon diodes, CR5 to CR8, are inserted in the control circuit. When the synthesizer is adjusted for a frequency within the range 0-1 MHz, the coil of the antenna relay K3 is fed from the 24-volt supply through the appropriate decade switches whereby the relay is energized, thus switching the antenna to the matching network for the medium-frequency range. The said decade switches also control the frequency-range selector relays in the power amplifier circuit so that the antenna matching network for the medium-frequency range is connected to the output of the power amplifier valve with the proper r.f. choke inserted in the anode circuit. When the synthesizer is adjusted for a frequency within the range 1-4 MHz, the coil of the antenna relay K2 is fed from the 24-volt supply through the diode CR6,7 and the appropriate decade switches whereby the relay is energized, thus switching the antenna to the matching network for the intermediate- and high-frequency range. The said decade switches also control the frequency-range selector relays in the power amplifier circuit so that the antenna matching network for the intermediate- and high-frequency range is connected to the output of the power amplifier valve with the proper r.f. choke inserted in the anode circuit. When the synthesizer is adjusted for a frequency within the range 4-7 MHz, or for a frequency within the range 7-30 MHz, the antenna relay K2 and the frequency-range selector relays in the power amplifier circuit are operated in a way similar to that described above, a separate r.f. choke being used for the range 7-30 MHz.

If the transmitter is installed in connection with an antenna switch unit with a built-in loading inductor for operation in the medium-frequency range, a keying interlock system should be used in order to prevent the transmitter from being operated in the intermediate- and high-frequency range when the loading inductor is switched into the antenna circuit. The antenna switch unit should be provided with an interlock switch which short-circuits the terminals designated "H.F. interlock" on the terminal board TB1 when the antenna switch is set in a position where the loading inductor is inserted in series with the antenna. When these terminals are short-circuited the transmitter cannot be keyed if the synthesizer is adjusted for a frequency within the range 1-30 MHz.

A muting relay, K1, located on the rear plate of the cabinet rack, provides means for muting associated receivers during transmission. When the key contacts are closed the coil of the

relay K1 is fed from the 24-volt d.c. supply through the diode CR1, while when the press-to-talk switch on the handset is closed the relay coil is fed from the 24-volt d.c. supply through the diode CR2. The change-over contacts of the relay K1 are brought out to the terminals designated "Muting" on the terminal board TB1. The output terminals of the 24-volt d.c. supply are brought out to the terminals designated "24V" on the terminal board TB1. This supply may be used for the external muting circuit, if required.

Two blowers are provided for forced ventilation of the transmitter, the blower B1 mounted in the rear plate of the cabinet rack and the blower A4B1 mounted in the power amplifier assembly. These blowers are fed from a 220-volt a.c. supply located in the main power supply assembly and are started when the transmitter is switched on by means of the switch designated "start" on the front panel of the s.s.b. exciter.

2.2.3. Main Power Supply Assembly. Reference Designation A1.

This assembly contains a 3-kV d.c. anode supply for the power amplifier stage, a 220-volt d.c. screen-grid supply and regulator for the power amplifier stage, a 24-volt d.c. supply for control circuits, relays, etc., a 220-volt a.c. supply, an overload-control circuit for the power amplifier stage, two timer circuits, a push-button switch and two thermally-operated circuit breakers.

The anode-voltage rectifier CR1, which consists of 36 silicon diodes, is fed from the mains through the delta-star connected power transformer T2. The rectifier output voltage is smoothed through the filter consisting of the inductor L1 and the capacitor C1. A bleeder resistor, R5, is provided across the filter output to improve the voltage regulation and to discharge the filter capacitor when a panel-and-chassis assembly is withdrawn. The 3-kV d.c. output voltage from the filter is applied to the anode circuit of the power amplifier stage. The resistor R4 is used as a shunt resistor for the anode current meter.

The screen-grid voltage rectifier A1A2CR1 is fed from the mains through the power transformer T4. The rectifier output voltage is filtered and applied to a series regulator, the output voltage of which can be adjusted within 200V to 250V by means of the potentiometer A1A2R7. The stabilized output voltage is applied to the screen-grid circuit of the power amplifier stage through the contacts on the relay A1A2K1, which contacts are shunted by the resistor A1A2R9 so that this resistor is inserted in series with the screen grid when the relay contacts are open. The relay A1A2K1 is controlled by the overload-control circuit, which employs three transistors, A1A1Q7,Q8,Q9. The coil of the relay A1A1K3 is inserted in the collector circuit of the output transistor Q9. The overload-control circuit is thermally-operated by means of a temperature-sensing device consisting of a thermistor, A4RT1, mounted on the anode connector of the power amplifier valve. This thermistor is inserted in a resistance bridge connected to the differential input of the overload-control circuit, so that if the temperature of the power amplifier valve anode exceeds the rated value, the overload-control circuit causes the relay A1A2K1 to open its contacts whereby the resistor A1A2R9 is inserted in series with the screen grid, thus reducing the voltage to spare the valve. An indicator lamp, designated "overload", on the power-amplifier control panel is switched on by an extra contact set on the relay A1A1K3 to indicate that the power amplifier is overloaded. The potentiometer A1A2R7 is preadjusted for a zero-signal power amplifier anode current of 300 mA d.c. Note that reference is made to the zero-signal anode current and not the screen-grid voltage. The adjustment of this potentiometer should be checked if the power amplifier valve is replaced by a new valve.

The 24-volt rectifier CR2 is fed from the mains through the power transformer T3. This transformer has a separate winding which provides a 220-volt a.c. "primary" supply for the power amplifier heater transformer and other low-power transformers in the transmitter. A filter capacitor, C2, a bleeder resistor, R6, and a fuse, F1, are provided in the output circuit of the rectifier CR2. The fuse F1 is accessible for replacement when the front panel and the screen in front of the rectifier assembly is removed. The rectifier provides a 24-volt d.c. supply for control circuits, relays, indicator lamps, etc. in the main power supply assembly as well as in other parts of the transmitter.

Two timers are incorporated in the circuit, a one-minute timer employing three transistors A1A1Q1,Q2,Q3, and a relay A1A1K1, and a three-minute timer employing three transistors, A1A1Q4,Q5,Q6, and a relay, A1A1K2. These timers are inserted in the start and stand-by control circuits of the transmitter in order to prevent the anode and screen-grid voltages from being switched to the power amplifier valve before the heater is warmed up. The time delay of the one-minute timer is mainly determined by the resistance-capacitance combination A1A1R9,C1 while the time delay of the three-minute timer is mainly determined by resistance-capacitance combination A1A1R21,C2,C3. When the transmitter is stopped the capacitors in the time-delay circuits are short-circuited by means of contact sets on the relays K1 and K3 whereby the output relays A1A1K1 and A1A1K2 are kept de-energized.

The transmitter is started by means of a push-button switch assembly located on the front panel. This switch assembly has two push-buttons designated "stand by" and "start". The equipment is protected by means of two thermally-operated circuit breakers, CB1 for the low-voltage supplies, and CB2 for the high-voltage supplies, i.e. the anode and screen-grid supplies. The circuit breakers are provided with bimetal switches which break the circuit when the current exceeds a predetermined value, 2.0 A for CB1 and 4.6 A for CB2. The bimetal switches are reset from the front panel by means of two push-buttons designated "reset"-"lt" and "ht". The relay contacts of the circuit breakers are operated by means of coils designed for 24-volt a.c. operation. The relay of the circuit breaker CB 1 is controlled by means of the standby-start switch assembly. The relay of the circuit breaker CB2 is controlled by means of the standby-start switch assembly, the relays K1,K2 and K3, the timers, the interlock switch S2 and the interlock switches for the other panel-and-chassis assemblies. For these interlock switches, see section 2.1 in this manual. The coils of the circuit-breaker relays and the relays K1,K2 and K3 are fed from the 24-volt secondary winding on the transformer T1, the primary winding of this transformer being connected directly to the mains, i.e. to the line voltage of the three-phase system.

When the stand-by push-button is pressed, the short-circuit connection is removed from the capacitors A1A1C2,C3 by means of the relay K1 and power is applied to the transformer T3 by means of the circuit breaker CB1 so that the heater of the power amplifier valve is warmed up. After a duration of approximately three minutes the relay A1A1K2 is energized, but since the relay A1A1K1 remains de-energized, no power is applied to the anode and screen-grid supplies. If the start push-button is then pressed, the short-circuit connection is removed from the capacitor A1A1C1 by means of the relay K3. After a duration of approximately one minute the relay A1A1K1 is energized, whereby the relay K2 is also energized and power is then applied to the anode and screen-grid supplies by means of the circuit breaker CB2. If the transmitter is started directly by means of the start push-button without using the stand-by push-button, power is immediately applied to the transformer T3, and after a duration of approximately three minutes power is also applied the anode and screen-grid supplies. When the stand-by push-button is pressed, after the transmitter has been started by means of the start push-button, the transmitter is switched into the stand-by condition described above. Two indicator lamps are provided on the front panel, DS1, designated "stand by", and DS2, designated "on". The lamp DS1 is lighted when the transmitter is switched to the stand-by condition, and the lamp DS2 is lighted when the anode and screen-grid power supplies are switched on.

The power transformers T1, T2, T3 and T4 are provided with taps for operation on either 380V or 440V. It should be noted that the taps on all these transformers (three taps on the transformer T2) must be set for the correct operating voltage.

2.2.3. Main Power Supply Assembly. Reference Designation A1. x)

This assembly contains a 3-kV d.c. anode supply for the power amplifier stage, a 220-volt d.c. screen-grid supply and regulator for the power amplifier stage, a 24-volt d.c. supply for control circuits, relays, etc., a 220-volt a.c. supply, an overload-control circuit for the power amplifier stage, a timer circuit, a push-button switch and two thermally-operated circuit breakers.

The anode-voltage rectifier CR1, which consists of 36 silicon diodes, is fed from the mains through the delta-star connected power transformer T2. The rectifier output voltage is smoothed through the filter consisting of the inductor L1 and the capacitor C1. A bleeder resistor, R5, is provided across the filter output to improve the voltage regulation and to discharge the filter capacitor when a panel-and-chassis assembly is withdrawn. The 3-kV d.c. output voltage from the filter is applied to the anode circuit of the power amplifier stage. The resistor R4 is used as a shunt resistor for the anode current meter.

The screen-grid voltage rectifier A1A2CR1 is fed from the mains through the power transformer T4. The rectifier output voltage is filtered and applied to a series regulator, the output voltage of which can be adjusted within 200V to 250V by means of the potentiometer A1A2R7. The stabilized output voltage is applied to the screen-grid circuit of the power amplifier stage through the contacts on the relay A1A2K1, which contacts are shunted by the resistor A1A2R9 so that this resistor is inserted in series with the screen grid when the relay contacts are open. The relay A1A2K1 is controlled by the overload-control circuit, which employs three transistors, A1A1Q2,Q3,Q4. The coil of the relay A1A1K2 is inserted in the collector circuit of the output transistor Q2. The overload-control circuit is thermally-operated by means of a temperature-sensing device consisting of a thermistor, A4RT1, mounted on the anode connector of the power amplifier valve. This thermistor is inserted in a resistance bridge connected to the differential input of the overload-control circuit, so that if the temperature of the power amplifier valve anode exceeds the rated value, the overload-control circuit causes the relay A1A2K1 to open its contacts whereby the resistor A1A2R9 is inserted in series with the screen grid, thus reducing the voltage to spare the valve. An indicator lamp, designated "overload", on the power-amplifier control panel is switched on by an extra contact set on the relay A1A1K2 to indicate that the power amplifier is overloaded. The potentiometer A1A2R7 is preadjusted for a zero-signal power amplifier anode current of 300 mA d.c. Note that reference is made to the zero-signal anode current and not the screen-grid voltage. The adjustment of this potentiometer should be checked if the power amplifier valve is replaced by a new valve.

The 24-volt rectifier CR2 is fed from the mains through the power transformer T3. This transformer has a separate winding which provides a 220-volt a.c. "primary" supply for the power amplifier heater transformer and other low-power transformers in the transmitter. A filter capacitor, C2, a bleeder resistor, R6, and a fuse, F1, are provided in the output circuit of the rectifier CR2. The fuse F1 is accessible for replacement when the front panel and the screen in front of the rectifier assembly is removed. The rectifier provides a 24-volt d.c. supply for control circuits, relays, indicator lamps, etc. in the main power supply assembly as well as in other parts of the transmitter.

The transmitter is started by means of a push-button switch assembly located on the front panel. This switch assembly has two push-buttons designated "stand by" and "start". The equipment is protected by means of two thermally-operated circuit breakers, CB1 for the low-voltage supplies, and CB2 for the high-voltage supplies, i.e. the anode and screen-grid supplies. The circuit breakers are provided with bimetal switches which break the circuit when the current exceeds a predetermined value, 2.0 A for CB1 and 4.6 A for CB2. The bimetal switches are reset from the front panel by means of two push-buttons designated "reset"-"lt" and "ht". The relay contacts of the circuit breakers are operated by means of coils designed for 24-volt a.c. operation. The relay of the circuit breaker CB1 is controlled by means of the standby-start switch assembly. The relay of the circuit breaker CB2 is controlled by means

x) See footnote on page 2-13A

of the standby-start switch assembly, the relays K1,K2 and K3, a special timer circuit, the interlock switch S2 and the interlock switches for the other panel-and-chassis assemblies. For these interlock switches, see section 2.1 in this manual. The coils of the circuit-breaker relays and the relays K1,K2 and K3 are fed from the 24-volt secondary winding on the transformer T1, the primary winding of this transformer being connected directly to the mains, i.e. to the line voltage of the three-phase system. The above-mentioned special timer circuit consists mainly of a dual-nand TTL Schmitt trigger, IC1, which operates as a multivibrator, three 4-bit binary counters, IC5,IC6 and IC7, and a latching circuit, IC2,IC3 and IC4. The frequency of the multivibrator is approximately 17 Hz.

When the stand-by push-button is pressed, the short-circuit connection is removed from the terminals "13" and "14" on the subassembly A1A1 by means of the relay K1, the counters are operated and power is applied to the transformer T3 by means of the circuit breaker CB1 so that the heater of the power amplifier valve is warmed up. After a duration of approximately two minutes the latch IC3 changes over and the input "11" on IC4 goes high, but since the terminal "9" on the subassembly A1A1 remains connected to ground the counter circuit is blocked again and no power is applied to the anode and screen-grid supplies. If the start push-button is then pressed, the short-circuit connection is removed from the terminal "9" and ground by means of the relay K3. After a duration of approximately one minute the relay A1A1K1 is energized, whereby the relay K2 is also energized and power is then applied to the anode and screen-grid supplies by means of the circuit breaker CB2. If the transmitter is started directly by means of the start push-button without using the stand-by push-button, power is immediately applied to the transformer T3, and after a duration of approximately three minutes power is also applied the anode and screen-grid supplies. When the stand-by push-button is pressed, after the transmitter has been started by means of the start push-button, the transmitter is switched into the stand-by condition described above. Two indicator lamps are provided on the front panel, DS1, designated "stand by", and DS2, designated "on". The lamp DS1 is lighted when the transmitter is switched to the stand-by condition, and the lamp DS2 is lighted when the anode and screen-grid power supplies are switched on.

The power transformers T1, T2, T3 and T4 are provided with taps for operation on either 380V or 440V. It should be noted that the taps on all these transformers (three taps on the transformer T2) must be set for the correct operating voltage.

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x) See diagram No.4215. Serial No.71332 and higher.

2.2.4. Single-Sideband Exciter Panel-and-Chassis Assembly. Reference Designation A2.

This panel-and-chassis assembly is designed to house up to eight plug-in modules or subassemblies (Ref. Designations A2A2 to A2A9) which are connected to the chassis wiring of the s.s.b. exciter through p.c. card connectors located on a common mother board. One subassembly (Ref. Designation A2A1) is connected to the chassis wiring and the mother-board wiring by means of soldered terminals and wires. Connections between the plug-in modules or subassemblies and the cabinet wiring or other panel-and-chassis assemblies are made by means of flexible cables and plugs and sockets on the module panels. A power transformer, T1, providing two 10-volt a.c. supplies and one 28-volt a.c. supply is located on the chassis frame. A push-button switch assembly, S1, used as a type-of-emission selector is mounted on the front panel, the push-buttons being designated "A1", "A2H", "F1", "A3H", "A3J", "simplex" and "duplex". On the front panel are also located a power-control potentiometer, R1, designated "power", and a test key, S2, and an indicator lamp, DS1, designated "test". The complete circuit diagram of the s.s.b. exciter panel-and-chassis assembly wiring is located in the diagram section of this manual together with the circuit diagrams of the plug-in modules and subassemblies.

2.2.4.1. Radio-Frequency Filter Circuits for External Wiring. Reference Designation A2A1.

Radio-frequency filters are provided at all terminals for the external power-supply wires and control wires to the s.s.b. exciter. The screening box containing these filter circuits is mounted on a standard module front panel which is fastened to the chassis frame of the s.s.b. exciter in a way similar to that used for the plug-in modules. The external wires are connected to the filter circuits by means of a plug which is inserted in a socket, J1, on the module front panel. The filter circuits are interconnected with the chassis wiring by means of soldered terminals. Some of the filter circuits are provided with zener diodes, CR1 to CR8, in order to protect the control circuits in question against overvoltage, especially the control circuits in which transistor-transistor logic gates are used.

2.2.4.2. S.S.B. Exciter Power Supply. Reference Designation A2A2.

The plug-in module containing this power supply is located in the s.s.b. exciter drawer. The complete power supply consists of a 10-volt rectifier supplying a +5-volt stabilized output, a 10-volt rectifier supplying a -5-volt stabilized output, and a 28-volt rectifier supplying a +24-volt stabilized output. The rectifiers are fed from the transformer T1 mounted on the s.s.b. exciter chassis, and since each voltage-stabilized power supply is fed from a separate rectifier connected to a separate winding on the power transformer, the positive or the negative output terminal of a power supply may be grounded at choice. In the +24-volt supply and in the +5-volt supply the negative terminal is grounded, while in the -5-volt supply the positive terminal is grounded.

Circuitry for the +5V and -5V supplies is identical and the description following is valid for both supplies:

10 volts ac from the print-board connector, pins 5, 6 (3, 4) are applied to full-wave bridge rectifier, CR101 (CR102). The ripple-DC output of the bridge is filtered by smoothing capacitors C101, C102 (C104, C105) and fed to the input of voltage regulator IC101 (IC102). Regulated DC output (5V) is shunted by bypass capacitor C103 (C109) and fed to pin M (pin K) on the print board connector.

+24V supply: 28 volts ac input to the +24V supply is drawn at pins 1 and 2 on the print board connector and applied to full-wave bridge rectifier CR103. Output of the bridge is filtered by smoothing capacitors C107, C108 and fed to pin 1 of voltage regulator IC103. The voltage regulator's through-return is connected to 1.8 k-ohm resistor, R102 which is itself connected in parallel with series wired zener diodes, CR104, CR105. Upon power supply activation, approximately 5V, regulated, is developed across 300 ohm resistor, R101 resulting in a current flow of approx. 17 mA through resistor R102 and a consequent voltage drop across the series connected zener diodes. The zener diodes will go on (forward conduct) and pull the voltage across R102 down to approx. 19V. Thus a total of 5V plus 19V will appear across bypass capacitor C109 and therewith, pin 1 of the print board connector.

2.2.4.3. Audio-Frequency Signal Processing Circuits. Reference Designation A2A3.

The plug-in module containing the audio-frequency signal processing circuits is located in the s.s.b. exciter drawer. The complete circuit diagram is located in the diagram section at the rear of this manual. The circuit diagram can be divided into seven sections:- A tune and A2H-emission oscillator, an audio-frequency channel selector, an audio-frequency amplifier, a clipper, a low-pass filter, and a sidetone oscillator and keyer.

The tune and A2H-emission oscillator is an R-C coupled oscillator employing two transistors, Q1 and Q2. The oscillator frequency is approximately 700 Hz. It will be seen from the circuit diagram that the series-coupled elements in the feedback circuit are resistive, while the shunt-coupled elements are capacitive. The feedback path is actually a low-pass filter so that an output signal having a relatively low distortion can be obtained from this filter at the point where the second and the third sections are joined. This output signal is applied to a buffer amplifier transistor, Q3. The output signal from this buffer amplifier is applied to a variable attenuator consisting of the resistor R20 and the junction field-effect (J-FET) transistor Q7 which is operated as a voltage-controlled resistor. The oscillator is controlled from the function control circuit (Ref. Designation A2A8) by means of the control line designated "Osc.". When this line goes "high" (logic level "1") the oscillator is started, and simultaneously the audio-frequency channel-selector transistor Q4 is saturated. The transistor Q4 controls the a.f. channel-selector gates IC1A to IC1D so that when the said transistor is saturated the outputs of the gates IC1C and IC1D go "low" (logic level "0"). These gates control the J-FET transistors Q5 and Q6, which are analogue switches. The output signal from the externally connected microphone is applied to the variable attenuator, R20,Q7, through the potentiometer R13, the capacitor C7 and the J-FET transistor Q5, while the output signal from an externally connected tone-shift oscillator (F1), if provided, is applied to the variable attenuator through the potentiometer R12, the capacitor C8 and the J-FET transistor Q6. When the oscillator is started the analogue switches Q5 and Q6 are kept open, because the outputs of the gates IC1C and IC1D are low so that only the 700-Hz signal from the tune and A2H-emission oscillator is applied to the variable attenuator.

The a.f. channel-selector gates IC1A to IC1D are also controlled from the function control circuit by means of the control line designated "Channel". When the control line designated "Osc." is low the transistor Q4 is cut off, i.e. the logic level of its collector is high. If in this case the control line designated "Channel" goes high, the analogue switch Q5 will close and switch the signal from the microphone to the variable attenuator, while if the said control line goes low the analogue switch Q6 will close and switch the signal from the external tone-shift oscillator to the variable attenuator. The circuit is so arranged that only one of the three a.f. signal sources, the tune and A2H-emission oscillator, the microphone or the tone-shift oscillator, can be switched to the variable attenuator at a time.

The output signal from the variable attenuator, R20,Q7, is applied to an a.f. amplifier employing three of the transistors in the integrated circuit IC2. The fourth transistor in this cir-

cuit is used as a detector for the output signal from the a.f. amplifier, the a.f. signal being applied to the base of the transistor and to a rectifier, CR1. The collector of the detector transistor is connected to the base of a transistor, Q15, in the collector circuit of which is inserted a constant-current loading transistor, Q16. A capacitor, C24, is connected across the constant-current load in series with a resistor, R38. The d.c. voltage obtained across the capacitor C24 is applied to the base of the transistor Q7. It should be noted that the detector used in this compressor is not altogether a conventional rectifier circuit. The diode CR1 operates as an ordinary rectifier and is conducting when the output signal from the a.f. amplifier has a negative amplitude. But when the signal has a positive amplitude the detector transistor (terminals "6","7" and "8" on IC2) is operative and provides a current amplification so that the capacitor C24 is charged, and since the transistor Q16 provides a constant-current load (high d.c. impedance) the resulting d.c. control voltage across the capacitor C24 will reach a value of plus several volts even if the output signal from the a.f. amplifier is relatively low, say one volt peak-to-peak. The function of the capacitors C21 and C22 is similar to that of the capacitors in a conventional voltage-multiplying rectifier circuit. As long as the a.f. signal voltage applied to the detector is lower than the "opening voltage" for the diode CR1 and the base-emitter diode of the detector transistor, no d.c. control voltage is produced by the detector circuit, but as the a.f. signal is increased the said diodes become conductive and the detector and the following amplifier will then produce a d.c. control voltage which increases rapidly with the a.f. signal voltage. The gain of the compressor circuit depends on the d.c. level on the base of the transistor Q7, and varies inversely at this level over the compression range of 26 dB. Thus, the output signal level of the a.f. compressor circuit is maintained almost constant, within 0.5 dB, for an input signal level variation of 26 dB.

The output signal from the a.f. compressor amplifier is applied to a differential amplifier, IC3, via an a.f. amplifier, Q8. The differential-pair transistors are coupled as a voltage follower. This circuit is operated as a speech clipper, the clipping level being adjusted by means of the variable resistor R45 in the common emitter circuit for the two transistors. Due to the great amount of negative feedback in the circuit the function of the clipper is almost ideal; for signal voltages below the clipping level the circuit operates as a normal amplifier with very low distortion. The output signal from the clipper is attenuated and fed to another differential amplifier consisting of a Darlington-pair amplifier, which is contained in the integrated circuit IC3, and a common-base connected transistor, Q9. A low-pass filter, L3, C31,C32,C33,R52,R53, is inserted between the emitters of the Darlington-pair output transistor and the transistor Q9, the relatively low terminating impedance being convenient for the filter design. The output signal from the transistor Q9 is applied to the balanced modulator (Ref. Designation A2A4), the proper output signal level being pre-adjusted by means of the potentiometer R54.

The transmitter may be used in connection with either a carbon microphone or a dynamic microphone. Separate input terminals are provided for the two types of microphone, the socket contacts J1-"1" and J1-"2" for a carbon microphone and J1-"2" and J1-"3" for a dynamic microphone. In the case of a carbon microphone a d.c. current of approximately 50 mA for the microphone is obtained from the +5-volt supply. The microphone signal level for the input to the a.f. compressor circuit is pre-adjusted by means of the potentiometer R13. Input terminals, socket contacts J1-"4" and J1-"5", for the connection of an external tone-shift oscillator for "F1" operation are also provided in the circuit. The signal level for this input is pre-adjusted by means of the potentiometer R12.

The sidetone oscillator is an R-C coupled oscillator employing two transistors, Q11 and Q12. The oscillator frequency is approximately 700 Hz. The output signal from the oscillator is amplified by the transistor Q13 and applied to the external circuit, e.g. the a.f. input circuit of a receiver associated with the transmitter, through the analogue switch consisting of the J-FET transistor Q14. This transistor is controlled from the function control circuit through the control line designated "Sidetone Key" in such a way that when this line is low, no sig-

nal is applied to the external circuit, while when this line is high the 700-Hz signal is applied to the external circuit, i.e. the sidetone is present when the key is closed. The sidetone oscillator is controlled from the function control circuit through the control line designated "Sidetone" in such a way that the sidetone oscillator is switched on only when the type-of-emission selector is set for A1 or A2 operation, or when the frequency synthesizer is set for transmission on 500 kHz.

2.2.4.4. Modulator, Filter and Mixer Circuits. Reference Designation A2A4.

The plug-in module containing the p.c. card for these circuits is located in the s.s.b. exciter drawer. The complete circuit diagram is located in the diagram section at the rear of this manual. This diagram can be divided into ten individual circuits:- A balanced modulator circuit, a l.s.b. crystal filter circuit, a carrier reinsertion circuit, a balanced mixer circuit, a 34.9991-35.0000 MHz amplifier circuit, a two-crystal l.s.b. filter circuit, a second balanced mixer circuit, a low-pass filter circuit, an output amplifier circuit, and a pulse-shaping and keying circuit.

The balanced modulator employs an integrated circuit, IC1, with three transistors. In this modulator the output signal obtained from the audio-frequency amplifier circuit (Ref. Designation A2A3) modulates a 1.5-MHz carrier signal to produce a double-sideband signal with suppressed carrier. The 1.5-MHz carrier signal, which is obtained from the frequency standard (Ref. Designation A3A3), is applied to the modulator through a transformer, T2, the signal level being determined by the type-of-emission selector and the carrier reinsertion circuit. The use of a centre-tapped transformer, T1, in the output circuit of the modulator allows the 1.5-MHz carrier signal to be balanced out. The modulator is followed by a crystal filter, FL1, which selects the lower sideband of the output signal from the modulator and provides further suppression of the carrier.

The carrier reinsertion circuit, which is connected to the secondary winding of the transformer T2, provides means for reinsertion of the 1.5-MHz carrier signal at the input of the first balanced mixer along with the l.s.b. signal from the crystal filter output. The carrier reinsertion signal is obtained from the arm of a potentiometer, R7, which is fed from the secondary wind-winding of the transformer T2. The level of the carrier signal applied to the potentiometer depends on which of the two ends of the winding or which of the two taps is ground-connected. Four switching diodes, CR1 to CR4, are provided in the circuit for ground-connecting the proper winding end or tap. These switching diodes are controlled by the function control circuit and the type-of-emission selector. The potentiometer R7 is adjusted to provide the correct carrier signal level when the transmitter is operated with the type-of-emission selector on A3H, in which case the switching diode CR3 at the centre-tap of the transformer winding is conducting. The circuit is so designed that when the carrier reinsertion signal for A3H operation has been preadjusted for the correct level, the different signal levels for the other types of emission will also be correct, while the peak amplitude of the resulting input signal to the mixer is held at its proper level independent of the selected type of emission.

The first balanced mixer employs an integrated circuit, IC2, with three transistors. In this mixer the l.s.b. signal from the output of the crystal filter FL1, which signal may also include a reinserted 1.5-MHz signal, is mixed with a variable-frequency signal of 33.4991-33.5000 MHz to produce a new l.s.b. signal with a carrier frequency equal to 1.5-MHz plus the actual frequency of the variable-frequency input signal. The variable-frequency input signal to the mixer is obtained from the 33.4991-33.5000 MHz phase-locked loop in the synthesizer (Ref. Designation A3A4). The d.c. bias on the base of the transistor in the mixer to which this signal is applied (terminal "12") is controlled within the range -5V to 0V by means of a potentiometer, A2R1, located on the front panel of the s.s.b. exciter and designated "power control". The above mentioned transistor is used as a variable-gain amplifier, and by means of the potentiometer the level of the output signal from the mixer can be controlled within the range from zero to full output. The use of a centre-tapped transformer

winding in the output tuned circuit, T4,C22, of the mixer allows the 33.4991-33.5000 MHz signal to be balanced out. The carrier frequency of the l.s.b. signal from the mixer will lie within the range 34.9991-35.000 MHz, the actual frequency being determined by the setting of the 1st decade switch in the synthesizer.

The l.s.b. output signal from the first mixer is amplified by a transistor, Q1, and applied to the second mixer through a two-crystal l.s.b. filter circuit. This filter is designed as a one-section half-lattice filter with extended bandwidth. Proper balance of the circuit is obtained by means of the adjustable differential capacitor C29. The second mixer is a double-balanced mixer employing two transformers and four diodes in a ring circuit, T6,CR5,T8. The l.s.b. signal from the output of the crystal filter is mixed with a variable-frequency signal, which is obtained from the 35.000-64.999 MHz phase-locked loop (Ref. Designation A3A6) in the synthesizer, to produce an u.s.b. signal with a carrier frequency equal to the difference between the frequency of the signal from the synthesizer and the carrier frequency of the l.s.b. input signal to the mixer. The phase-locked signal from the synthesizer is applied to the mixer via a transistor amplifier, Q2, and a transformer, T7. The carrier frequency of the upper-sideband signal obtained from the output of the mixer will lie within the range 0-29.9999 MHz, the actual frequency being determined by the setting of the decade switches in the synthesizer. The output signal from the mixer is applied to an emitter follower, Q3, through a low-pass filter, L10,L11,C36-C38, which rejects the undesired sum-frequency signal from the mixer. The output signal from the emitter follower is applied to a three-stage wide-band amplifier (Ref. Designation A2A5) through p.c. card-edge connectors.

The pulse-shaping and keying circuit employs three transistors, Q4, Q5 and Q6. The keying contact in the function control circuit is connected to the base of the transistor Q4 through the resistor R29. The "power control" potentiometer A2R1 on the front panel of the s.s.b. exciter is connected between the collector of the transistor Q6 and the -5-volt supply lead, so that when no current flows through the transistor Q6 the variable-gain transistor in the first mixer is cut off. When the transmitter is keyed the keying contact in the function control circuit goes to logic level 0, whereby the base voltage on the transistor Q4 is altered so that this transistor is saturated. The pulse-shaping capacitors C43 and C44 will then be charged whereby the transistors Q5 and Q6 will be conducting, and the collector current of the transistor Q6 will pass through the "power control" potentiometer and provide the proper operating bias for the variable-gain transistor in the first mixer, thus keying the transmitter. In order to limit the collector current of the transistor Q6 to a suitable value, a voltage-amplitude limiter employing the diodes CR6 to CR9 is provided in the input circuit of the transistor Q5. The shapes of the pulse leading and trailing edges of the keying pulses are mainly determined by the capacitors C43 and C44 and the resistors R28 and R32.

2.2.4.5. Three-Stage Wide-Band Amplifier. Reference Designation A2A5.

This amplifier, which is contained in a plug-in module, consists of a three-stage wide-band amplifier preceded by a low-pass filter. This low-pass filter, the input of which is connected to the output of the modulator filter and mixer circuits (Ref. Designation A2A4) in the s.s.b. exciter through p.c. card-edge connectors, allows signals of frequencies within the range 400 kHz to 30 MHz to be passed on to the wide-band amplifier and provides further suppression of the undesired signals from the mixer. The wide-band amplifier employs three transistors, Q1, Q2 and Q3. The output signal from the wide-band amplifier is applied to the following two-stage wide-band amplifier (Ref. Designation A2A7) through a coaxial cable. If required, a special filter may be inserted in the coaxial-cable connection between these two wide-band amplifier, see below.

2.2.4.6. Noise Suppressor Filter Circuit. Reference Designation A2A6.

This filter circuit is contained in a plug-in module fitted with two coaxial-cable sockets so that it can, if required, be inserted in the coaxial-cable connection between the two wide-band amplifiers mentioned above. The filter circuit consists of six individual circuits for suppression of noise at frequencies within those parts of the 4-, 6-, 8-, 12-, 16- and 22-MHz maritime bands for telephony on which a receiver associated with the transmitter may be operated.

2.2.4.7. Two-Stage Wide-Band Amplifier. Reference Designation A2A7.

This amplifier, which amplifies the output signal from the three-stage wide-band amplifier (Ref. Designation A2A5), is also contained in a plug-in module. It employs two transistors, Q1 and Q2. The output stage provides an output power of approximately 1 watt p.e.p. into 50Ω (approximately 20 V peak-to-peak). The output signal is fed through a coaxial cable to a driver (Ref. Designation A4A1) preceding the power amplifier stage of the transmitter.

2.2.4.8. Function Control Circuit. Reference Designation A2A8.

The subassembly containing this circuit is located on the wiring side of the mother board in the s.s.b. exciter drawer, the interconnections being made by means of p.c. card-to-card connectors. The functions which are controlled by means of the function control circuit are listed below. The reference designations added (in brackets) to the function descriptions in the list refer to the designations used in the circuit diagram for the gate inputs and outputs and corresponding control lines in question.

1. Selection of the proper a.f. channel, ("Channel").
2. Selection of the proper key, ("Key out").
3. On and Off switching of the sidetone oscillator, ("Sidetone act.").
4. Keying of the sidetone oscillator, ("Sidetone key").
5. Selection of the carrier reinsertion ratio, ("H", "A", "J", "J'").
6. On and Off switching of the tune and A2H-emission oscillator, ("Osc.").

These functions are controlled in accordance with the information received from the following control circuits:-

a. The inputs from the type-of-emission selector, ("A1", "A2H", "F1", "A3H", "A3A", "A3J", - only one of these control lines being low at a time), and the input from the simplex-duplex switch, ("K1").

b. The input from the "tune" switch on the power amplifier panel, ("tune").

c. The inputs from the frequency synthesizer decade switches, ("500 kHz", "2182 kHz").

d. The inputs from the key interlocking switches located in the antenna matching network assemblies, ("Key interlocking").

e. The inputs from the keys, ("K1", "K2").

All the gates used in the function control circuit are of the integrated-circuit type. The input circuits which are controlled by simple ground-connecting switches are provided with pull-up resistors, R1 to R13, one for each input, so that these inputs are kept at a level of +5 V (logic level "1", or "high") when their control lines are not switched to ground (the grounded control line corresponds to logic level "0", or "low"). The truth table for the function control circuit is shown on the following page, Table 2.2.4.8-1.

Table 2.2.4.8-1. Truth Table for the Function Control Circuit.

Input x)										500 kHz = 0 2182 kHz = 1										500 kHz = 1 2182 kHz = 0										500 kHz = 1 2182 kHz = 1									
										Output																													
F1	A1	A2H	A3H	A3A	A3J	K1	K2	Tune		J'	J	A	H	Osc.	Channel	Key out (xx	Sidet. key	Sidet. act.		J'	J	A	H	Osc.	Channel	Key out (xx	Sidet. key	Sidet. act.		J'	J	A	H	Osc.	Channel	Key out (xx	Sidet. key	Sidet. act.	
0	1	1	1	1	1	0	0	0		1	1	1	0	1	0	0	1	1		1	1	1	0	1	1	0	1	0		1	0	1	1	1	0	0	1	0	
0	1	1	1	1	1	1	0	0		1	1	1	0	1	0	0	1	1		1	1	1	0	1	1	0	1	0		1	0	1	1	1	0	0	1	0	
0	1	1	1	1	1	0	1	0		1	1	1	0	1	0	0	1	1		1	1	1	0	1	1	0	1	0		1	0	1	1	1	0	0	1	0	
0	1	1	1	1	1	1	1	0		1	1	1	0	1	0	0	1	1		1	1	1	0	1	1	0	1	0		1	0	1	1	1	0	0	1	0	
0	1	1	1	1	1	0	0	1		1	1	1	0	1	0	0	1	1		1	1	1	0	0	1	0	1	0		1	0	1	1	0	0	0	1	0	
0	1	1	1	1	1	1	0	1		1	1	1	0	1	0	1	0	1		1	1	1	0	0	1	0	1	0		1	0	1	1	0	0	0	1	0	
0	1	1	1	1	1	0	1	1		1	1	1	0	1	0	0	1	1		1	1	1	0	0	1	1	1	0		1	0	1	1	0	0	0	1	0	
0	1	1	1	1	1	1	1	1		1	1	1	0	1	0	1	0	1		1	1	1	0	0	1	1	1	0		1	0	1	1	0	0	0	1	0	
1	0	1	1	1	1	0	0	0		1	1	1	0	1	1	0	1	1		1	1	1	0	1	1	0	1	1		0	1	1	1	1	1	0	1	1	
1	0	1	1	1	1	1	0	0		1	1	1	0	1	1	0	1	1		1	1	1	0	1	1	0	1	1		0	1	1	1	1	1	0	1	1	
1	0	1	1	1	1	0	1	0		1	1	1	0	1	1	0	1	1		1	1	1	0	1	1	0	1	1		0	1	1	1	1	1	0	1	1	
1	0	1	1	1	1	1	1	0		1	1	1	0	1	1	0	1	1		1	1	1	0	1	1	0	1	1		0	1	1	1	1	1	0	1	1	
1	0	1	1	1	1	0	0	1		1	1	1	0	1	1	0	1	1		1	1	1	0	0	1	0	1	1		0	1	1	1	0	1	0	1	1	
1	0	1	1	1	1	1	0	1		1	1	1	0	1	1	1	0	1		1	1	1	0	0	1	0	1	1		0	1	1	1	0	1	1	0	1	
1	0	1	1	1	1	0	1	1		1	1	1	0	1	1	0	1	1		1	1	1	0	0	1	1	1	1		0	1	1	1	0	1	0	1	1	
1	0	1	1	1	1	1	1	1		1	1	1	0	1	1	1	0	1		1	1	1	0	0	1	1	1	1		0	1	1	1	0	1	1	0	1	
1	1	0	1	1	1	0	0	0		1	1	1	0	1	1	0	1	1		1	1	1	0	1	1	0	1	1		1	1	1	0	1	1	0	1	1	
1	1	0	1	1	1	1	0	0		1	1	1	0	1	1	0	1	1		1	1	1	0	1	1	0	1	1		1	1	1	0	1	1	0	1	1	
1	1	0	1	1	1	0	1	0		1	1	1	0	1	1	0	1	1		1	1	1	0	1	1	0	1	1		1	1	1	0	1	1	0	1	1	
1	1	0	1	1	1	1	1	0		1	1	1	0	1	1	0	1	1		1	1	1	0	1	1	0	1	1		1	1	1	0	1	1	0	1	1	
1	1	0	1	1	1	0	0	1		1	1	1	0	1	1	0	1	1		1	1	1	0	0	1	0	1	1		1	1	1	0	1	1	0	1	1	
1	1	0	1	1	1	1	0	1		1	1	1	0	1	1	1	0	1		1	1	1	0	0	1	0	1	1		1	1	1	0	1	1	0	1	1	
1	1	0	1	1	1	0	1	1		1	1	1	0	1	1	0	1	1		1	1	1	0	0	1	1	1	1		1	1	1	0	1	1	0	1	1	
1	1	0	1	1	1	1	1	1		1	1	1	0	1	1	1	0	1		1	1	1	0	0	1	1	1	1		1	1	1	0	1	1	0	1	1	
1	1	1	0	1	1	0	0	0		1	1	1	0	1	1	0	1	1		1	1	1	0	1	1	0	1	0		1	1	1	0	1	1	0	1	0	
1	1	1	0	1	1	1	0	0		1	1	1	0	1	1	0	1	1		1	1	1	0	1	1	0	1	0		1	1	1	0	1	1	0	1	0	
1	1	1	0	1	1	0	1	0		1	1	1	0	1	1	0	1	1		1	1	1	0	1	1	0	1	0		1	1	1	0	1	1	0	1	0	
1	1	1	0	1	1	1	1	0		1	1	1	0	1	1	0	1	1		1	1	1	0	1	1	0	1	0		1	1	1	0	1	1	0	1	0	
1	1	1	0	1	1	0	0	1		1	1	1	0	1	1	0	1	1		1	1	1	0	0	1	0	1	0		1	1	1	0	0	1	0	1	0	
1	1	1	0	1	1	1	0	1		1	1	1	0	1	1	1	0	1		1	1	1	0	0	1	1	1	0		1	1	1	0	0	1	0	1	0	
1	1	1	0	1	1	0	1	1		1	1	1	0	1	1	1	0	1		1	1	1	0	0	1	1	1	0		1	1	1	0	0	1	1	1	0	
1	1	1	0	1	1	1	1	1		1	1	1	0	1	1	1	0	1		1	1	1	0	0	1	1	1	0		1	1	1	0	0	1	1	1	0	
1	1	1	1	0	1	0	0	0		1	1	1	0	1	1	0	1	1		1	1	1	0	1	1	0	1	0		1	1	0	1	1	1	0	1	0	
1	1	1	1	0	1	1	0	0		1	1	1	0	1	1	0	1	1		1	1	1	0	1	1	0	1	0		1	1	0	1	1	1	0	1	0	
1	1	1	1	0	1	0	1	0		1	1	1	0	1	1	0	1	1		1	1	1	0	1	1	0	1	0		1	1	0	1	1	1	0	1	0	
1	1	1	1	0	1	1	1	0		1	1	1	0	1	1	0	1	1		1	1	1	0	1	1	0	1	0		1	1	0	1	1	1	0	1	0	
1	1	1	1	0	1	0	0	1		1	1	1	0	1	1	0	1	1		1	1	1	0	0	1	0	1	0		1	1	0	1	0	1	0	1	0	
1	1	1	1	0	1	1	0	1		1	1	1	0	1	1	1	0	1		1	1	1	0	0	1	1	1	0		1	1	0	1	0	1	0	1	0	
1	1	1	1	0	1	0	1	1		1	1	1	0	1	1	1	0	1		1	1	1	0	0	1	1	1	0		1	1	0	1	0	1	0	1	0	
1	1	1	1	0	1	1	1	1		1	1	1	0	1	1	1	0	1		1	1	1	0	0	1	1	1	0		1	1	0	1	0	1	0	1	0	
1	1	1	1	1	0	0	0	0		1	1	1	0	1	1	0	1	1		1	1	1	0	1	1	0	1	0		1	0	1	1	1	1	0	1	0	
1	1	1	1	1	0	1	0	0		1	1	1	0	1	1	0	1	1		1	1	1	0	1	1	0	1	0		1	0	1	1	1	1	0	1	0	
1	1	1	1	1	0	0	1	0		1	1	1	0	1	1	0	1	1		1	1	1	0	1	1	0	1	0		1	0	1	1	1	1	0	1	0	
1	1	1	1	1	0	0	1	1		1	1	1	0	1	1	0	1	1		1	1	1	0	0	1	0	1	0		1	0	1	1	0	1	0	1	0	
1	1	1	1	1	0	1	0	1		1	1	1	0	1	1	1	0	1		1	1	1	0	0	1	0	1	0		1	0	1	1	0	1	0	1	0	
1	1	1	1	1	0	0	1	1		1	1	1	0	1	1	0	1	1		1	1	1	0	0	1	1	1	0		1	0	1	1	0	1	1	1	0	
1	1	1	1	1	0	1	1	1		1	1	1	0	1	1	1	0	1		1	1	1	0	0	1	1	1	0		1	0	1	1	0	1	1	1	0	

x) The input circuits are controlled by simple ground-connecting switches, i.e. the ground connection corresponds to logic level "0".

xx) If the input "Key interlocking" is "0" the output "Key out" is "1" (unconditionally).

2.2.4.9. Automatic Fault Localization Device. Reference Designation A2A9.

The automatic fault localization (a.f.l.) device is supplied on special request. The subassembly containing this device is designed to be located in the s.s.b. exciter drawer and connected to the mother board wiring by means of p.c. card-to-card connectors. The complete a.f.l. circuit can be divided into seven individual circuits, i.e. six signal-sensing circuits and a fault-localizing circuit.

In order to check the operation of the s.s.b. exciter the six signal-sensing circuits are connected to appropriate circuits contained in the plug-in modules. If the circuit being checked operates properly the signal-sensing circuit in question provides an output signal of logic level 1, but in case of faulty operation the signal-sensing circuit provides an output signal of logic level 0. The outputs of the signal-sensing circuits are connected to the inputs of the fault-localizing circuit through the test points designated "C", "D", "E", "F", "H" and "K" in the circuit diagram. The signal-sensing circuits for the inputs "H" and "K" are contained in the wide-band amplifier modules (Ref. Designations A2A5 and A2A7). The signal sources to be checked are:-

Test Point:	Signal source:	Ref. Designation of the plug-in module:
"C"	-5-volt regulated output from power supply	A2A2
"D"	+28-volt regulated output from power supply	A2A2
"E"	Output from a.f. signal processing circuits	A2A3
"F"	0.4-30 MHz output from modulator, filter and mixer circuits	A2A4
"H"	0.4-30 MHz output from three-stage wide-band amplifier	A3A5
"K"	0.4-30 MHz output from two-stage wide-band amplifier	A3A7

The fault-localizing circuit has five outputs, one for each plug-in module. To each output is connected a transistor in the emitter circuit of which is inserted an indicator lamp. The output signals from the signal-sensing circuits are applied simultaneously to the fault-localizing circuit. If the s.s.b. exciter operates properly the outputs from the signal-sensing circuits will all be at logic level 1, and none of the indicator lamps mentioned above will light. If the circuit in a plug-in module fails to operate properly the output from the signal-sensing circuit concerned will be at logic level 0, and the fault-localizing circuit will cause the indicator lamp for the plug-in module in question to light, thus indicating in which plug-in module the faulty circuit is localized. Similarly, if faults occur in two or more plug-in modules simultaneously, the indicator lamps for all the faulty modules will be lighted. The indicator lamps for the plug-in modules are located on top of the subassembly containing the a.f.l. device so that they are visible when the s.s.b. exciter drawer is withdrawn. An extra indicator lamp, which is located on the front panel and designated "test", is lighted when a fault occurs in a plug-in module, but in order to find out where the fault is localized the s.s.b. exciter drawer must be withdrawn so that the indicator lamps for the plug-in modules are visible.

The a.f.l. device for the s.s.b. exciter is switched on by means of a push-button switch which is located on the front panel and designated "test".

The principle of operation of the a.f.l. device for the s.s.b. exciter is similar to that of the a.f.l. device for the frequency synthesizer, see paragraph 2.2.5.10.

2.2.5. Frequency Synthesizer Panel-and-Chassis Assembly. Reference Designation A3.

This panel-and-chassis assembly (drawer) is designed to house up to eight plug-in modules or subassemblies (Ref. Designations A3A1 to A3A8) which are connected to the chassis wiring of the synthesizer through p.c. card connectors located on a common mother board. An extra subassembly (Ref. Designation A3A9) is connected to the mother board wiring by means of soldered terminals and wires. Connections between the plug-in modules or subassemblies and the cabinet wiring or other panel-and-chassis assemblies are made by means of flexible cables and plugs and sockets on the module panels. A power transformer, T1, providing a 24-volt a.c. supply is located on the chassis frame. A switch assembly containing six decade switches, S1 to S6, is mounted on the chassis so that the switch knobs can be operated from the front panel. This assembly also contains two indicator lamps, DS1 ("distress") and DS2 ("test") which are visible from the front panel. The complete circuit diagram of the synthesizer chassis wiring is located in the diagram section at the rear of this manual together with the circuit diagrams of the plug-in modules and subassemblies.

It should be noted that the p.c. card-edge receptacles on the mother board and the p.c. card-edge contacts on the plug-in modules are so arranged that the row of contacts identified with numbers, starting with number "1", on a receptacle connect with the row of card-edge contacts on the component side of the p.c. card in the mating plug-in module, while the row of contacts identified with letters, starting with letter "A", on a receptacle connect with the row of card-edge contacts on the wiring side opposite the component side of the p.c. card in the mating module. Card-to-card connectors for a subassembly containing a gate-off circuit (Ref.Designation A3A8), or an automatic fault localization device (Ref. Designation A3A10), are provided on the wiring side of the mother board. A test-point jack, J10, and a potentiometer, R1, for adjustment of the standard-frequency oscillator are located on the component side of the mother board. These components are accessible through holes in the top cover.

The decade switch sections controlling the variable-ratio frequency dividers are binary-coded, the switch functions being performed in accordance with the truth tables shown on the circuit diagrams for the dividers (Ref. Designations A3A5 and A3A7). Extra switch sections are provided for other control circuits. The four control wires designated "0-1 MHz", "1-4 MHz", "4-7 MHz" and "7-30 MHz" interconnect the decade switches with the frequency-range selector relays in the power amplifier and antenna circuits, via the rectifier plug-in module, the flexible cable and the cabinet wiring. This control circuit is so arranged that the required switch functions for changing-over the power-amplifier and antenna circuits to the matching network for operation in the frequency range corresponding to the frequency setting of the synthesizer is automatically carried out by the said relays. The two control wires designated "0-1 MHz" and "1-4 MHz" are also connected to the 1.5-MHz signal-level control circuit (Ref. Designation A3A9).

The two control wires designated "500 kHz" and "2182 kHz" interconnect the decade switches and the type-of-emission selector circuit in the s.s.b. exciter via the diodes CR1 and CR4. This control circuit is so arranged that when the synthesizer is set for transmission on 500 kHz the s.s.b. exciter is unconditionally adjusted for A2H operation, and similarly, when the synthesizer is set for transmission on 2182 kHz the s.s.b. exciter is unconditionally adjusted for A3H operation. The indicator lamp DS1 is lighted when the synthesizer is set on 500 kHz or 2182 kHz, the lamp being fed from the 24-volt a.c. supply through the appropriate decade switch sections and a diode, CR2 (on 500 kHz) or CR3 (on 2182 kHz). The indicator lamp DS2 is connected to the gate-off circuit (Ref. Designation A3A8), or the automatic fault localization device (Ref. Designation A3A10), if provided.

2.2.5.1. Rectifier Circuits. Reference Designation A3A1.

The power supplies for the frequency synthesizer are contained in two plug-in modules, the rectifier circuits being contained in one module and the voltage-regulator circuits in the other. The two modules are located side by side in the synthesizer drawer. The complete circuit diagrams are located in the diagram section at the rear of this manual. The external primary-supply wires and control-circuit wires are connected to the synthesizer through the plug and socket P3,J1. Radio-frequency filters are provided at all terminals for the external wiring. The required supply voltages for the voltage-regulator-circuit module are provided by the transformer T1 and the rectifiers CR1 to CR4.

An extra voltage regulator for a -12-volt supply is provided in the output circuit of the rectifier CR2. It should be noted that this regulated supply of -12V will not be produced if the rectifier-circuit module is withdrawn from the mother board, or if the regulator-circuit module is withdrawn, because the output circuit of the rectifier CR2 obtains its ground connection from the regulator-circuit module so that this ground connection will not be present unless the said rectifier and the +12-volt regulator circuit are interconnected.

2.2.5.2. Voltage-Regulator Circuits. Reference Designation A3A2.

This plug-in module contains the voltage regulators for the power-supply rectifiers mentioned in the previous paragraph. The regulated power supplies are:- A +17-volt supply, a +12-volt supply, a +5-volt supply and a -5-volt supply. As mentioned in the previous paragraph a -12-volt regulator is contained in the rectifier-circuit module.

The +17-volt regulator circuit consists of two cascaded series regulators. The first regulator is a conventional series regulator with short-circuit protection, while the second regulator is a special regulator in which most of the component parts are contained in the integrated circuit IC1. This regulator, which is also a series regulator with short-circuit protection, provides the required extra high voltage stability for the +17-volt supply. The +12-volt, +5-volt and -5-volt regulators are conventional series regulators with short-circuit protection. Each of the four regulated power supplies is fed from a separate rectifier connected to a separate winding on the power transformer so that one of the output terminals of the regulator, the positive or the negative, may be grounded at choice. In the +17-volt, +12-volt and +5-volt regulators the negative terminal is grounded, while in the -5-volt regulator the positive terminal is grounded.

The shunt resistors R35, R23, R24, R25 and R26 are factory selected parts. Appropriate resistors are inserted in the circuits at the factory in order to obtain the correct output voltages from the regulators.

2.2.5.3. Frequency Standard. Reference Designation A3A3.

The plug-in module containing the frequency standard is located in the frequency synthesizer drawer. The complete circuit diagram is located in the diagram section at the rear of this manual. The circuit can be divided into seven sections:- A 7.5-MHz standard-frequency oscillator, an oven-control circuit, a pulse shaper, a fixed-ratio frequency divider, a 1.5-MHz amplifier, a frequency multiplier, and a 1.5-MHz control circuit.

The standard-frequency oscillator is a modified Pierce oscillator employing one of the transistors in the integrated circuit IC1. The principal frequency-controlling element consists of a 7.5-MHz crystal unit, Y1, with high frequency stability and low aging rate. A trimmer capacitor, C6, for coarse tuning and a pair of varactor diodes, CR1, for fine tuning of the oscillator are incorporated in the capacitive loading circuit for the crystal unit. The control-voltage for the varactor diodes is obtained from the arm of a potentiometer, A3R1, which is located on the mother board in the frequency synthesizer drawer and is accessible for adjustment by a screwdriver through a hole in the top cover. The potentiometer is fed from the stabilized 6-volt supply for the oscillator (through p.c. card-edge connector "B"). The collector of one of the four transistors in the integrated circuit, IC1, used for the oscillator is connected to the base to form a diode. This diode and the associated collector-to-substrate diode are connected as an amplitude limiter in the oscillator circuit. The two other transistors are used as buffer amplifiers for the 7.5-MHz oscillator output signal. The output signal from the first buffer amplifier is fed to a pulse shaper, Q1, which drives the fixed-ratio frequency divider, while the output signal from the second buffer amplifier is fed to the frequency multiplier.

The crystal unit and the oscillator circuitry are contained in a temperature-controlled oven with an operating temperature of 75°C. The heater winding, R22, is inserted in the output circuit of the oven-control output amplifier consisting of the Darlington-pair transistors Q3 and Q4. This amplifier, which is supplied directly from the unfiltered output of the 24-volt rectifier CR4, is controlled by a differential-input amplifier contained in the integrated circuit IC8. The 24-volt rectifier is supplied from a transformer, A3T1, in the synthesizer drawer. The temperature-sensing device consists of a thermistor, RT1, mounted on the outside of the inner chamber of the oven near the heater winding. The thermistor RT1 is inserted in a resistance bridge connected to the differential input of the integrated circuit IC8, the internal balanced resistor pair being used as one side of the bridge. The integrated circuit IC8 and the external side of the resistance bridge consisting of the thermistor RT1, the potentiometer R18 and the resistor R19 are fed from the 24-volt rectifier through a filter, CR5 and C24, and a voltage-stabilizing circuit, R17 and CR6. The oven temperature is preadjusted to its correct value, 75°C, by means of the potentiometer R18. The oven takes about four to five minutes to reach the proper temperature from 20°C ambient. Due to the time delay in heat transfer the oven-control system operates as a form of on-off proportional control, the heater winding normally being on for about 6 seconds and off for about 24 seconds when the ambient temperature is about 20°C. The oven cycle and its duty factor vary with the ambient temperature.

The 7.5-MHz output signal from the pulse shaper, Q1, is applied to the divide-by-five frequency divider contained in the integrated circuit IC2. The 1.5-MHz output signal from this divider is applied to the base of the transistor Q2, which is operated as a 1.5-MHz selective amplifier with a tuned circuit, L3,C16. The 1.5-MHz output signal obtained from the secondary winding of the transformer L3 is applied to the modulator circuit (Ref. Designation A2A4) in the s.s.b. exciter through a coaxial cable.

The output signal from the frequency divider IC2 is also applied to a divide-by-three frequency divider contained in the integrated circuit IC3. The 500-kHz signal from the Q output of the first J-K flip-flop in this divider is applied to a differentiating circuit, C18,R16, which produces appropriate multiples of the 500-kHz signal (n x 500 kHz) for checking the standard-frequency oscillator (the synthesizer frequency standard) against any suitable standard-

frequency transmission. To facilitate checking of the oscillator frequency the n x 500 kHz signal is brought out to a socket on the mother board in the synthesizer drawer. This socket is accessible through a hole in the top cover of the drawer. The 500-kHz output signal from the divider IC3 is applied to a frequency divider consisting of three cascaded decade dividers, IC4, IC5 and IC6, and a decoder gate, IC7. Most of the time during a complete division cycle the output of the gate IC7 is high (approx. +4.5V), but once during the cycle the output goes low for about 130 nanoseconds, i.e. negative-going output pulses are produced at a repetition rate of 500 per second. This signal is used as a 500-Hz reference signal and is applied to the two phase and frequency discriminators for the phase-locked loops (Ref. Designation A3A4 and A3A6).

The 7.5-MHz output signal from the second buffer amplifier in the standard-frequency oscillator circuit is applied to the input circuit of the frequency multiplier, which is tuned to 30 MHz. The frequency multiplier employs four transistors contained in the integrated circuit IC9. The 30-MHz output signal from the multiplier is applied to the balanced mixer in the 33.4991-33.5000 MHz loop plug-in module (Ref. Designation A3A4).

The output signal from the 1.5-MHz selective amplifier is also applied to a control circuit in which the signal is amplified and rectified. The rectified signal is then applied to an amplifier which provides means for driving a gate in a transistor-transistor logic circuit. The transistors used for amplification of the signal are contained in the integrated circuit IC10. The logic state of the output of the control circuit is high as long as the 1.5-MHz signal is present, and low when this signal disappears. The control circuit is intended for use in connection with an automatic fault localization device, which may be supplied on request.

2.2.5.4. 33.4991-33.5000 MHz Phase-Locked Loop.
Reference Designation A3A4.

The plug-in module containing this phase-locked loop circuit is located in the frequency synthesizer drawer. The complete circuit diagram is located in the diagram section at the rear of this manual. The circuit can be divided into seven sections:- A combined phase and frequency discriminator, a low-pass filter, a voltage-controlled crystal oscillator, a frequency multiplier, a balanced mixer, an output amplifier, and a special control circuit which may be used in connection with an automatic fault localization circuit.

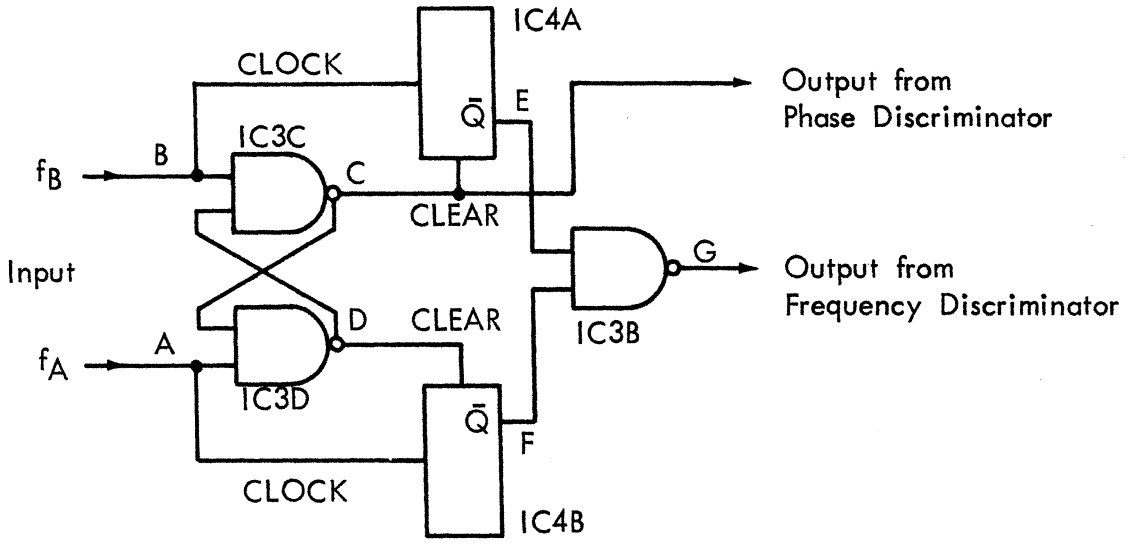
The 500-Hz reference-frequency signal obtained from the divider circuits in the standard-frequency oscillator assembly (Ref. Designation A3A3) is applied to the inputs of the flip-flop IC4A and the gate IC3C in the combined phase and frequency discriminator circuit. The output signal from the 33.4991-33.5000 MHz frequency divider circuit (Ref. Designation A3A5), which is to be compared with the 500-Hz reference-frequency signal, is applied to the inputs of the flip-flop IC4B and the gate IC3D in the combined phase and frequency discriminator circuit. The timing diagram of the discriminator is shown in Fig. 2.2.5.4-1.

From this timing diagram it will be seen that when a pulse (waveform B) appears at the input B of the flip-flop IC3C,IC3D the output C of this flip-flop goes high, while when a pulse (waveform A) appears at the input A the output C goes low. Consequently, the duty factor of the rectangular wave (waveform C) at the output C is proportional to the phase difference between the input pulses at A and B (the pulse at A lagging behind the pulse at B) so that the average d.c. voltage obtained at the output C is also proportional to the said phase difference, i.e. the transfer function is linear. The output C is connected to the reset (clear) terminal of the J-K flip-flop IC4A, the $\bar{Q}$ output of which flip-flop is indicated by E in the diagram. The output D of the flip-flop IC3C,IC3D is connected to the reset (clear) terminal of the J-K flip-flop IC4B, the $\bar{Q}$ output of which flip-flop is indicated by F in the diagram. The logic states of the $\bar{Q}$ outputs of the flip-flops IC4A and IC4B, the E and F outputs, depend on the relation between the frequency, f_A, of the signal applied to the input A and the frequency, f_B, of the signal applied to the input B.

If $f_A = f_B$, the $\bar{Q}$ outputs of the flip-flops IC4A and IC4B will be kept in state 1, i.e. E = 1 and F = 1. For instance, if a pulse appears at the input A of the flip-flop IC3C,IC3D while the output state of this flip-flop is C = 1 and D = 0, the flip-flop IC4B will not change state because D = 0, i.e. it will remain in state $\bar{Q}$=1 (F=1). But the flip-flop IC3C,IC3D will change state to C=0 and D=1, so that when the next pulse appears at the input B the flip-flop IC4A will not change state because C=0, i.e. it will remain in state $\bar{Q}$=1 (E=1). However, the flip-flop IC3C,IC3D will change state to C=1 and D=0, so that when a pulse appears at the input A again the above mentioned function will be repeated. Consequently, the outputs E and F will remain in state 1 as long as $f_A = f_B$.

If $f_A > f_B$, the time between the arrival of two consecutive pulses at the input A will be shorter than the time between the arrival of two consecutive pulses at the input B. Before long the situation will arise where two consecutive pulses arrive at the input A during the time between the arrival of two consecutive pulses at the input B. The first pulse appearing at the input A during this time will cause the flip-flop IC3C,IC3D to change state to C=0 and D=1. When the next pulse appears at the input A the flip-flop IC4B will change state to $\bar{Q}$=0, i.e. F=0, because the flip-flop IC3C,IC3D has remained in state C=0 and D=1. The flip-flop IC4B will remain in state $\bar{Q}$=0 until the next pulse appears at the input B. This pulse will cause the flip-flop IC3C,IC3D to change state to C=1 and D=0, thereby causing the flip-flop IC4B to change state to $\bar{Q}$=1, i.e. F=1. In this way pulses are produced at the output of the flip-flop IC4B (waveform F), the repetition rate being increased as the difference $f_A - f_B$ is increased.

If $f_A < f_B$, pulses are produced at the output of the flip-flop IC4A (waveform E) in a way similar to that described above, the circuit being symmetrical with respect to the inputs A and B.



f_A: Frequency of output signal from frequency divider.

f_B: Reference frequency.

The waveforms A to G shown below are the waveforms taken at the corresponding points shown in the circuit diagram of the combined phase and frequency discriminator to the left.

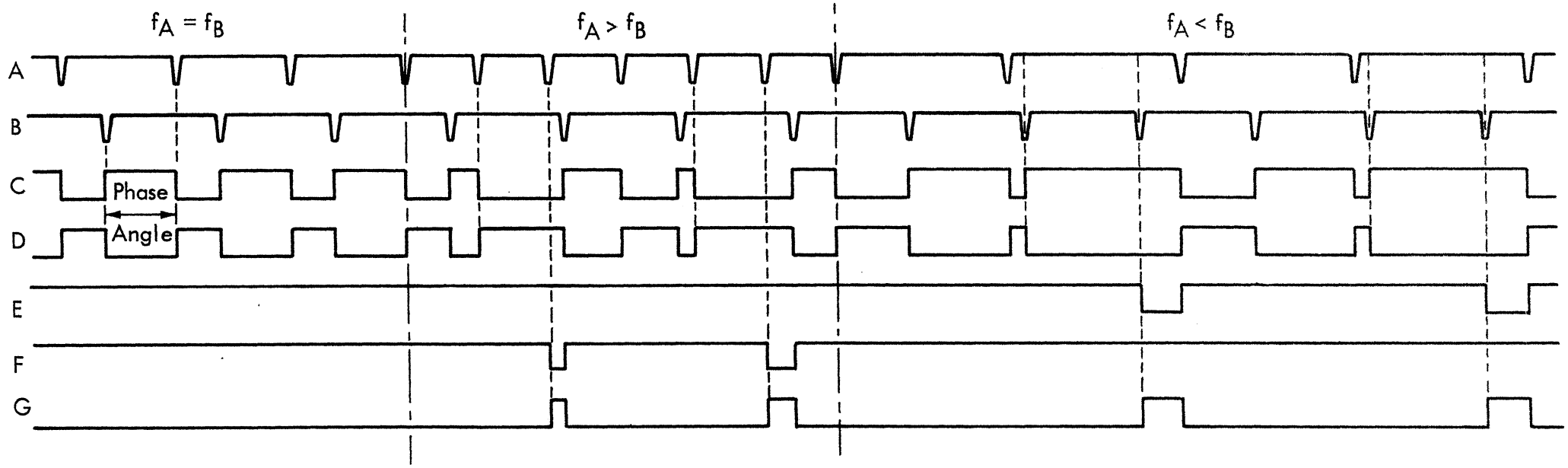


Fig. 2.2.5.4-1. Timing Diagram of Combined Phase and Frequency Discriminator.

The inputs of the gate IC3B are connected to the $\bar{Q}$ outputs of the flip-flops IC4A and IC4B, i.e. the E and F outputs. As long as $f_A = f_B$ the outputs E and F will remain in state 1 and the output G of the gate IC3B will then remain in state G=0. If $f_A \neq f_B$, pulses will appear at the output G of the gate IC3B as shown in waveform G. The output of the gate IC3B may be connected to an automatic fault localization device, if required.

The output signal from the phase discriminator gate IC3C is applied to the emitter of the transistor Q1 via the diode CR1. The purpose of the transistor Q1, which is fed from a stabilized 12-volt supply, is to provide output signals the logic levels of which remain constant even if the logic levels of the signals from the phase discriminator vary slightly. The output signal from the collector of the transistor Q1 is fed to the varactor diodes CR3 and CR4 in the oscillator tuning circuit through a low-pass filter.

The voltage-controlled crystal oscillator is a modified Pierce oscillator employing two transistors connected as a Darlington pair. The crystal Y1 is loaded by the inductor L2 and the varactor diodes CR3 and CR4 so that the oscillator frequency can be varied within the desired range from slightly below to slightly above the series resonant frequency of the crystal. The oscillator is preadjusted by means of the trimmer capacitors C8 and C9 to cover the required frequency range, 3.4991-3.5000 MHz, the actual frequency being determined by the d.c. voltage applied to the varactor diodes. The collector of one of the four transistors in the integrated circuit, IC1, used for the oscillator is connected to the base to form a diode. This diode and the associated collector-to-substrate diode are connected as an amplitude limiter in the oscillator circuit. The fourth transistor in the integrated circuit IC1 is employed as an amplifier for the output signal from the oscillator. The output signal from the collector circuit of this amplifier is applied to a multiply-by-five multiplier, while the output signal from the emitter circuit is applied to a balanced mixer.

The multiply-by-five frequency multiplier employs an integrated circuit, IC2, with four transistors. Appropriate filtering is provided by the two tuned circuits, L5,C18 and L6,C24. The output signal from the frequency multiplier, the frequency of which will lie within the range 17.4995-17.5000 MHz, is applied to the 33.4991-33.5000 MHz variable-ratio frequency divider (Ref. Designation A3A5). Division ratios of 34991, 34992, etc. to 35000 can be selected by the 1st decade switch on the synthesizer front panel. The output signal from the frequency divider is applied to the combined phase and frequency discriminator as described above and the loop is phase-locked on the frequency corresponding to the setting of the 1st decade switch.

The balanced mixer employs an integrated circuit, IC5, with three transistors. In this mixer the output signal from the voltage-controlled crystal oscillator is mixed with a 30-MHz signal, which is obtained from the standard-frequency oscillator assembly (Ref. Designation A3A3), to produce a signal with a frequency equal to the sum of the two input frequencies. The use of a centre-tapped inductor for the output tuned circuit allows the 30-MHz signal to be balanced out. The modulator output signal is applied to a tuned transistor amplifier, Q2, which is followed by an output amplifier consisting of a common-collector coupled transistor, Q3, (emitter follower). The output signal from the emitter circuit of this amplifier is applied to the modulator assembly (Ref. Designation A2A4) in the s.s.b. exciter via a coaxial cable. The frequency of this output signal will lie within the range 33.4991-33.5000 MHz, the actual frequency being determined by the setting of the 1st decade switch.

The output signal from the emitter follower is also applied to a control circuit in which the signal is amplified and rectified. The rectified signal is then applied to an amplifier which provides means for driving a gate in a transistor-transistor logic circuit. The transistors used for amplification of the signal are contained in the integrated circuit IC6. The logic state of the output of the control circuit is high as long as the 33.4991-33.5000 MHz signal is present, and low when this signal disappears. The control circuit is intended for use in connection with an automatic fault localization device, which may be supplied on request.

2.2.5.5. 33.4991-33.5000 MHz Variable-Ratio Frequency Divider. Reference Designation A3A5.

The plug-in module containing this divider is located in the frequency synthesizer drawer. The complete circuit diagram of the divider is located in the diagram section at the rear of this manual. As shown in the circuit diagram the plug-in module also contains a filter for a +5-volt supply, L1, C4 to C7, four pull-up resistors, R6 to R9, and a pulse shaper circuit, Q1, Q2 and ICE2D, which is inserted in the 17.4955-17.5000 MHz input to provide suitable clock pulses for a decade divider.

The variable-ratio frequency divider can be set to divide the frequency of the input signal, which will lie within the range 17.4955-17.5000 MHz, by any integer between 34991 and 35000, the division ratio being determined by the setting of the decade switch S1 ("0-0.9 kHz") on the frequency synthesizer front panel. The input signal is obtained from the frequency multiplier in the 33.4991-33.5000 MHz loop and mixer circuit (Ref. Designation A3A4). The frequency divider consists mainly of a synchronous decade divider, ICD2 to ICD6 and ICE2 to ICE4, which is controlled by the binary-coded decade switch S1 (connections "A1", "B1", "C1" and "D1"), and a 12-bit ripple-through binary divider, ICC4, ICB2 to ICB6, the division ratio of which is programmed by the decoder gates ICC2 and ICC3A to ICC3D.

The counting sequence for the divider is shown in Table 2.2.5.5-1. It should be noted that initially the Q outputs of the flip-flops in the decade divider and the $\bar{Q}$ outputs of the flip-flops in the ripple-through binary divider are all switched to state 0, and the flip-flop D2 is disabled by the flip-flop E2A,E2B and the gate E3C. The 8th input pulse in the count-by-ten sequence causes the flip-flop D3 to change state to Q=1 and $\bar{Q}$=0 whereby the flip-flops D4 and D5 are disabled, their Q outputs remaining in state 0. On the receipt of the 9th input pulse the outputs of the flip-flop D3 will not change state because one J input as well as one K input are in state 0. The 10th input pulse causes the flip-flop D3 to change state to Q=0 and $\bar{Q}$=1 again whereby the flip-flops D4 and D5 are enabled, thus restarting the counting sequence for the decade divider. The negative-going edge of the output pulse thus generated by the Q output of the flip-flop D3 triggers the first flip-flop C4A in the ripple-through binary divider.

When the ripple-through binary divider has counted the number of pulses corresponding to the programmed division ratio, i.e. 3498 pulses if the decade switch is in one of the positions "1" to "9" or 3499 pulses if the said switch is in position "0", the output of the decoder gate C2 goes low and the flip-flop E2A,E2B changes state, thus causing those flip-flops in the ripple-through binary divider which are in state $\bar{Q}$=0 to change state to $\bar{Q}$=1. After this the output of the gate C2 goes high again without affecting the state of the flip-flop E2A, E2B. The flip-flop D3 is disabled by the gate E3B while the flip-flop D2 is enabled by the gate E3C to operate instead of the flip-flop D3 when seven more input pulses have been counted by the decade divider. Thus, on the receipt of the next input pulse (the 34988th or the 34998th pulse) the flip-flop D3 remains in state Q=0 and $\bar{Q}$=1, the flip-flops D4 to D6 change state to Q=0 while the flip-flop D2 changes state to Q=1 and $\bar{Q}$=0. The output Q=1 of the flip-flop D2 enables the appropriate decoder gates, E4A to E4D, to set the decade divider in accordance with the decade switch position (the modified 'divider state') and causes the output of the gate E2C to go low, thus generating a negative-going output pulse which is applied to the phase discriminator in the 33.4991-33.5000 MHz loop and mixer circuit. The output $\bar{Q}$=0 of the flip-flop D2 disables the flip-flops D3 to D6 so that on the receipt of the following input pulse (the 34989th or the 34999th pulse) the flip-flop D2, the K inputs of which are permanently at state 1, changes state to Q=0 and $\bar{Q}$=1 whereby the output of the gate E2C goes high, the flip-flop E2A,E2B obtains its original state and the flip-flops D3 to D6 are enabled to count in accordance with the decade switch setting. The last input pulse in the counting sequence resets the decade divider to zero and causes the flip-flops in the ripple-through binary divider to change state to $\bar{Q}$=0, thus restarting the counting sequence.

The decade divider follows the 1-2-4-8 code. The 'divider state' to which it has to be set by the decade switch in order to obtain the desired division ratio corresponds to the complement to 9 of the number of extra input pulses n which has to be counted before the appropriate input pulse restarting the counting sequence is received. For the decade switch settings "1" to "9" the division ratio is equal to 3499x10+n. In the case where the decade switch is set to position "0" the ripple-through binary divider is programmed by the decoder gates C3A to C3D to count one more pulse from the decade divider before the decade divider is set to count in accordance with the decade switch setting, and since n=o the division ratio is equal to 3500x10+0 = 35000.

The principle of operation of the frequency synthesizer and the s.s.b. exciter is described in section 2.2.1. Block Diagram. The output signal from the 33.4991-33.5000 MHz loop and mixer circuit is mixed with a 1.5-MHz signal to produce an output signal within the frequency range 34.9991-35.0000 MHz, the actual output frequency being determined by the setting of the 1st decade switch. This signal is finally mixed with a signal in the frequency range 35.0000-64.9990 MHz to produce a difference-frequency output signal in the transmitting frequency range 0-29.9999 MHz. The actual frequency of the mixer input signal in the range 35.0000-64.9990 MHz is determined by the settings of the other decade switches. It will be seen that if the frequency in the range 34.9991-35.0000 MHz is increased the transmitting frequency is decreased, while if the frequency in the range 35.0000-64.9990 MHz is increased the transmitting is also increased. Therefore, the coding of the 1st decade differs from that of the other decades.

Table 2.2.5.5-1. Counting Sequence for 33.4991-33.5000 MHz Variable-Ratio Frequency Divider

Number of Counted Input Pulses and Corresponding 'Divider State'	Division Ratio	Output Frequency of Loop and Mixer Circuit (kHz)	Position of Decade Switch S1
Input Pulses → 1 2 3 4 5 6 7 8 9 10			
0 1 2 3 4 5 6 7 8 9	35000	33500.0	0
0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9	34999	33499.9	1
0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 [0] 0 1 2 3 4 5 6 7 8 9	34998	33499.8	2
0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 [1] 1 2 3 4 5 6 7 8 9 0	34997	33499.7	3
0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 [2] 2 3 4 5 6 7 8 9 0	34996	33499.6	4
0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 [3] 3 4 5 6 7 8 9 0	34995	33499.5	5
0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 [4] 4 5 6 7 8 9 0	34994	33499.4	6
0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 [5] 5 6 7 8 9 0	34993	33499.3	7
0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 [6] 6 7 8 9 0	34992	33499.2	8
0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 [7] 7 8 9 0	34991	33499.1	9
0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 [8] 8 9 0			

34970 34971 34972 34973 34974 34975 34976 34977 34978 34979 34980 34981 34982 34983 34984 34985 34986 34987 34988 34989 34990 34991 34992 34993 34994 34995 34996 34997 34998 34999 35000

Initially the Q outputs of the flip-flops in the decade divider and the $\bar{Q}$ outputs of the flip-flops in the ripple-through binary divider are all switched to state 0. From the start of the counting sequence and until the ripple-through binary divider has counted the number of pulses corresponding to its programmed division ratio, the decade divider operates as a divide-by-ten divider. For every ten input pulses the decade divider generates an output pulse which is applied to the input of the ripple-through binary divider.

When the 34980th input pulse (switch positions "1" to "9") or the 34990th input pulse (switch position "0") has been counted the output of the gate C2 goes low and the flip-flop E2A, E2B changes state, thus causing the $\bar{Q}$ outputs of the flip-flops in the ripple-through binary divider to go to state 1. Simultaneously the flip-flop D3 in the decade divider circuit is replaced by the flip-flop D2 so that the decade divider can be set to count in accordance with the position of the decade switch.

The state is modified according to the position of the decade switch. When this state is reached the output of the gate E2C goes low, thus generating a negative-going output pulse which is applied to the phase discriminator in the 33.4991-33.5000 MHz loop and mixer circuit. The last input pulse in the counting sequence resets the decade divider and causes the flip-flops in the ripple-through binary divider to change state to $\bar{Q} = 0$, thus restarting the counting sequence.

2.2.5.6. 35.000-64.999 MHz Phase-Locked Loop. Reference Designation A3A6.

The plug-in module containing this loop circuit is located in the frequency synthesizer drawer. The complete circuit diagram is located in the diagram section at the rear of this manual. The circuit can be divided into ten sections: - A combined phase and frequency discriminator, an 8-bit up-down counter, a 2-bit binary to one-of-four decoder, a digital-to-analogue converter, a low-pass filter, a voltage-controlled oscillator, an output amplifier, and three voltage regulators for power supplies.

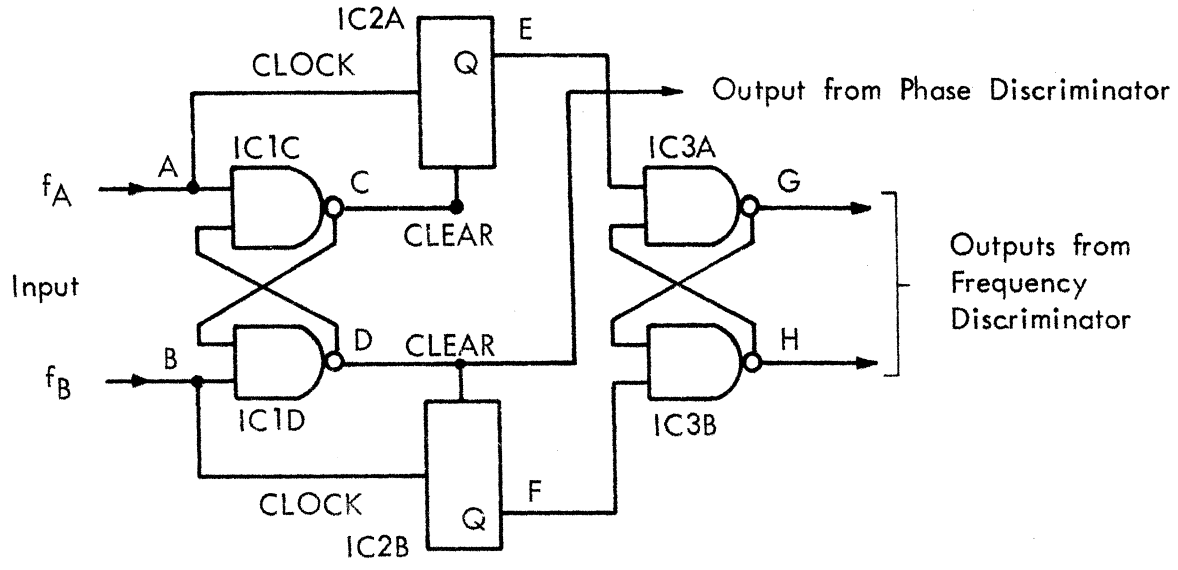
The 500-Hz reference-frequency signal obtained from the divider circuits in the standard-frequency oscillator assembly (Ref. Designation A3A3) is applied to the inputs of the flip-flop IC2B and the gate IC1D in the combined phase and frequency discriminator circuit. The output signal from the 35.000-64.999 MHz frequency divider circuit (Ref. Designation A3A7), which is to be compared with the 500-Hz reference-frequency signal, is applied to the inputs of the flip-flop IC2A and the gate IC1C in the phase and frequency discriminator circuit through the interface circuit Q37,C44,R86,R88 and the driver gates IC1A and IC1B. The timing diagram of the phase and frequency discriminator is shown in Fig. 2.2.5.6-1.

From this timing diagram it will be seen that when a pulse (waveform B) appears at the input B of the flip-flop IC1C,IC1D the output D of this flip-flop goes high, while when a pulse (waveform A) appears at the input A the output D goes low. Consequently, the duty factor of the rectangular wave (waveform D) at the output D is proportional to the phase difference between the input pulses at A and B (the pulse at A lagging behind the pulse at B) so that the average d.c. voltage obtained at the output D is also proportional to the said phase difference, i.e. the transfer function is linear. The output C of the flip-flop IC1C,IC1D is connected to the reset (clear) terminal of the J-K flip-flop IC2A, the Q output of which flip-flop is indicated by E in the diagram. The output D is connected to the reset (clear) terminal of the J-K flip-flop IC2B, the Q output of which flip-flop is indicated by F in the diagram. The logic states of the Q outputs of the flip-flops IC2A and IC2B, the E and F outputs, depend on the relation between the frequency, f_A , of the signal applied to the input A and the frequency, f_B , of the signal applied to the input B.

If $f_A = f_B$, the Q outputs of the flip-flops IC2A and IC2B will be kept in state 0, i.e. E=0 and F=0. For instance, if a pulse appears at the input A of the flip-flop IC1C,IC1D while the output state of this flip-flop is C=0 and D=1, the flip-flop IC2A will not change state because C=0, i.e. it will remain in state Q=0 (E=0). But the flip-flop IC1C,IC1D will change state to C=1 and D=0, so that when the next pulse appears at the input B the flip-flop IC2B will not change state because D=0, i.e. it will remain in state Q=0 (F=0). However, the flip-flop IC1C,IC1D will change state to C=0 and D=1 so that when a pulse appears at the input A again, the above mentioned functions will be repeated. Consequently, the outputs E and F will remain in state 0 as long as $f_A = f_B$.

If $f_A > f_B$, the time between the arrival of two consecutive pulses at the input A will be shorter than the time between the arrival of two consecutive pulses at the input B. Before long the situation will arise where two consecutive pulses arrive at the input A during the time between the arrival of two consecutive pulses at the input B. The first pulse appearing at the input A during this time will cause the flip-flop IC1C,IC1D to change state to C=1 and D=0. When the next pulse appears at the input A the flip-flop IC2A will change state to Q=1, i.e. E=1, because the flip-flop IC1C,IC1D has remained in state C=1 and D=0. The flip-flop IC2A will remain in state Q=1 until the next pulse appears at the input B. This pulse will cause the flip-flop IC1C,IC1D to change state to C=0 and D=1, thereby causing the flip-flop IC2A to change state to Q=0, i.e. E=0. In this way pulses are produced at the output of the flip-flop IC2A (waveform E), the pulse repetition rate being increased as the difference $f_A - f_B$ is increased.

If $f_A < f_B$, pulses are produced at the output of the flip-flop IC2B (waveform F) in a way similar to that described above, the circuit being symmetrical with respect to the inputs A and B.



f_A: Frequency of output signal from frequency divider.

f_B: Reference frequency.

The waveforms A to H shown below are the waveforms taken at the corresponding points shown in the circuit diagram of the combined phase and frequency discriminator to the left.

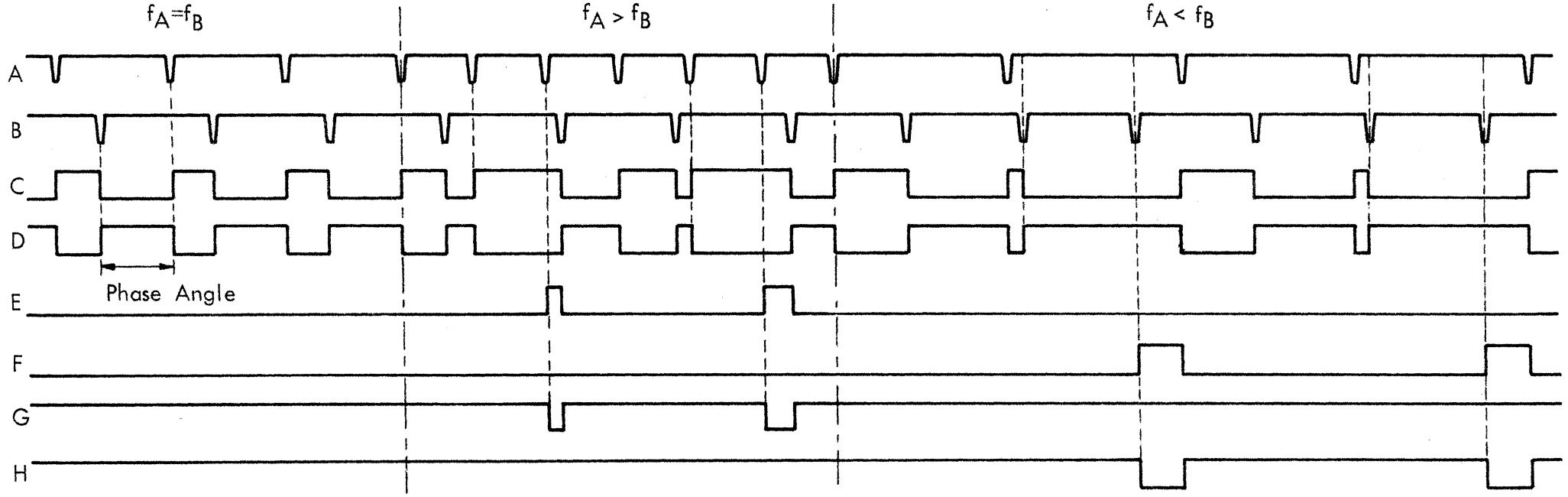


Fig. 2.2.5.6-1. Timing Diagram of Combined Phase and Frequency Discriminator.

The output signals from the flip-flops IC2A and IC2B are applied to the inputs of the flip-flop IC3A,IC3B which operates as an inverter. Input pulses of waveform E cause pulses of waveform G to be produced at output G of gate IC3A, while input pulses of waveform F cause pulses of waveform H to be produced at output H of gate IC3B. As long as the pulses at the inputs A and B of the flip-flop IC1C,IC1D do not appear simultaneously, the discriminator will operate as described above. But, since the duration of the pulses is finite, the situation may arise where the outputs of the flip-flops IC2A and IC2B go high simultaneously. However, only one of the outputs G and H can go low at a time because the two gates IC3A and IC3B are cross-coupled to form an R-S flip-flop circuit. The G and H outputs are connected to two cascaded 4-bit binary up-down counters, the output G being connected to the count-up terminal and the output H being connected to the count-down terminal of the first 4-bit counter.

The up-down counter consists of two MSI (medium-scale integrated circuit) 4-bit binary counters, IC4 and IC5. The carry output of the first counter is connected to the count-up terminal of the second counter while the borrow output of the first counter is connected to the count-down terminal of the second counter, so that the circuit forms an 8-bit binary up-down counter. The six least significant bits of this counter control a digital-to-analogue converter. The two most significant bits, the 7th bit and the 8th bit, control the circuit for selecting the proper tap on the oscillator inductor L4. A "load" (data strobe) control circuit, C45,Q38, Q39,Q40,R89, is provided in the output circuit of the 7th stage of the up-down (U/D) counter. This "load" control circuit is so arranged that every time the 7th bit is changed the positive-going or negative-going output pulse edge thus produced by the 7th U/D counter stage will cause the "load" terminal to go low for about three microseconds, and the 5th bit and the 6th bit will then change from 0 and 0 to 1 and 0, or from 1 and 1 to 1 and 0. The 7th bit and the 8th bit will not be changed because the data inputs of the 7th and 8th stages of the U/D counter are connected to their respective Q outputs. These stages will remain in the states they reached when the oscillator inductor tap was selected until the 7th bit is changed again in order to select another inductor tap. As mentioned above, the U/D counter is set to a condition different from the full or the empty condition every time the 7th bit is changed, i.e. when the oscillator inductor tap is selected. This is a very important function, and the reason for using such an arrangement will be explained later. The taps on the oscillator inductor L4 are selected by means of the four switching diodes CR11 to CR14, which are controlled by the 2-bit binary to one-of-four decoder circuit. The four decoder gates IC6A,to IC6D in this circuit are connected to the outputs of the 7th and 8th stages of the U/D counter through the gates IC3C and IC3D.

The digital-to-analogue (D/A) converter is used to coarse-tune the voltage-controlled oscillator. It translates the binary information obtained from the outputs of the first six stages of the U/D counter into an analogue information, i.e. a d.c. voltage, which is applied to the varactor diodes in the oscillator tuning circuit through a low-pass filter. All six stages in the D/A converter are equal except for the resistance values of the resistors R35 to R41. These values are: R35 = 2xR36, R36 = 2xR38, .. R39 = 2xR41. A simplified circuit diagram of the oscillator control circuit in which only two D/A converter stages are included is shown in Fig. 2.2.5.6-2. The transistors and diodes in the D/A converter circuits perform the function of connecting the resistors R35 to R41 to the 10-kΩ resistor R28 in different combinations so that the d.c. voltage, i.e. the analogue information, at the output of the D/A converter corresponds to the binary information at the input, see the table in Fig. 2.2.5.6-3. If the output of the first U/D counter stage (the least significant bit) is Q=0, the current drawn by the n-p-n transistor Q17 will cause the base voltage of the p-n-p transistor Q6 to fall so that the last-mentioned transistor will be saturated. The collector voltage of the transistor Q6 will then be approximately +12V, and since the output voltage from the D/A converter (the voltage between the point K and the common lead in Fig. 2.2.5.6-2) is equal to or lower than +12V the diode CR3 will be cut off. If the output of the first U/D counter stage is Q=1 the transistor Q17 will be cut off, thereby causing the transistor Q6 to be cut off, too.

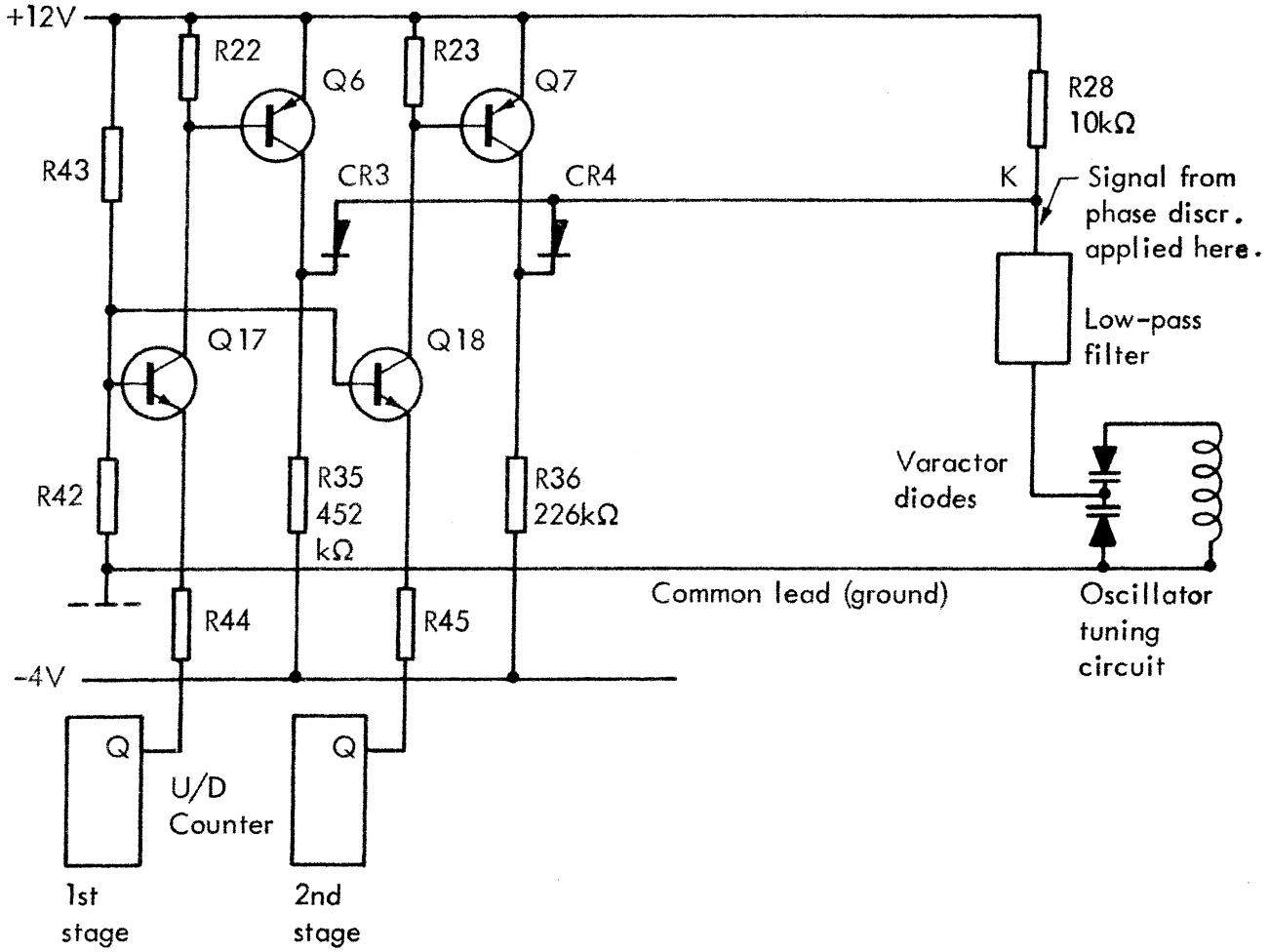


Fig. 2.2.5.6-2. Simplified Oscillator Control Circuit Diagram. Only two D/A converter stages are shown.

The diode CR3 will then be conducting and a current will flow from the +12V lead through the 10-kΩ resistor R28, the diode CR3, and the 452-kΩ resistor R35 to the -4V lead. This current will cause a voltage drop of 0.35V in the 10-kΩ resistor R28, i.e. the output voltage from the D/A converter will be 11.65V.

The other stages in the D/A converter will operate in a way similar to that described above for the first stage. From the table in Fig. 2.2.5.6-3 it will be seen that a 2-bit D/A converter provides means for varying the output voltage in four steps. The equivalent circuits show that the operation performed when a bit is changed (one step) is equivalent to connecting, or disconnecting, a 452-kΩ resistor across the "lower" part of the voltage divider in the output circuit of the D/A converter. It will be seen that when the U/D counter counts up, i.e. the step number is increased, the output voltage is decreased, while when the U/D counter counts down, i.e. the step number is decreased, the output voltage is increased. A graph representing the output voltage as a function of the step number of the U/D counter is shown in Fig. 2.2.5.6-4. When the characteristics of the varactor diodes are taken into consideration it will be seen that the graph mentioned above has the desired curvature for meeting the requirements of a constant servo-loop gain.

The actual 6-bit D/A converter provides means for varying the output voltage in 64 steps (2^6 steps). If the oscillator frequency is not brought inside the capture range of the loop by means of the control voltage available within the 64-step range, another tap on the oscillator inductor will automatically be selected by means of the two last stages in the U/D counter as described above. Thus, if the oscillator frequency is too low or too high, the U/D

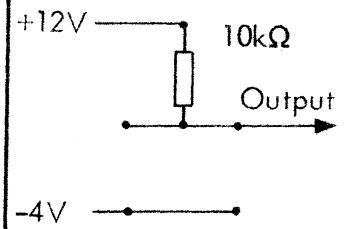
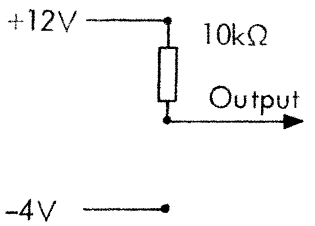
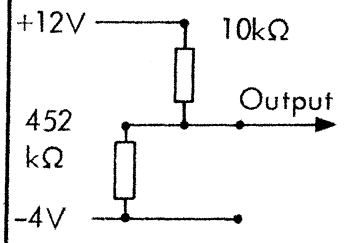
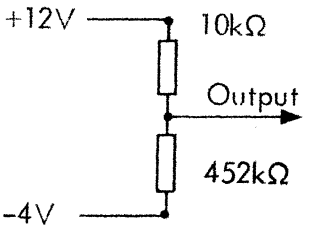
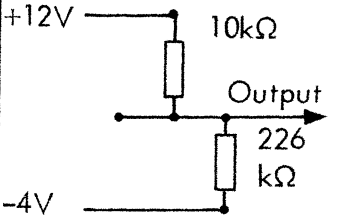
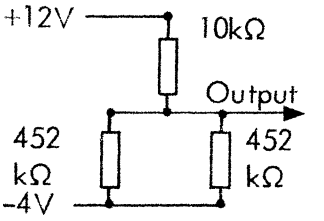
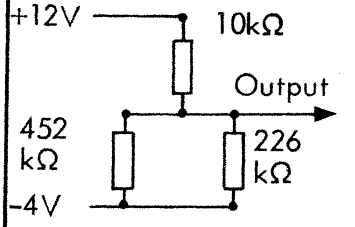
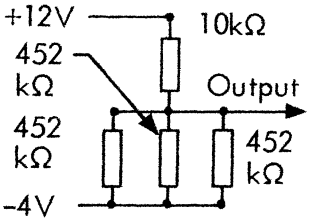
Step No.	Q Output of 1st U/D Counter Stage (least significant bit)	Q Output of 2nd U/D Counter Stage (next significant bit)	D/A Converter Output Circuit		
			Actual Circuit	Equivalent Circuit	Output Voltage (Volts)
0	0	0			12.00
1	1	0			11.65
2	0	1			11.32
3	1	1			11.02

Fig. 2.2.5.6-3. Principle of Operation of D/A Converter. Only two stages are shown.

counter will count down or up, respectively, until the oscillator frequency is brought inside the capture range of the loop so that the phase locking can be established. A graph representing the oscillator frequency as a function of the step number of the U/D counter is shown in Fig. 2.2.5.6-5.

The output signal from the phase discriminator gate IC1D is applied to the emitter of the transistor Q2 via the diode CR1. The purpose of the transistor Q2 is to provide output signals the logic levels of which remain constant even if the logic levels of the signals from the phase discriminator vary slightly. The output signal from the collector of the transistor Q2 is fed to the input of the low-pass filter through the resistor R6 and added to the output signal from the D/A converter. It should be noted that the signal from the phase discriminator is attenuated in a voltage divider, the "upper" part of which consists of the resistor R6 while the "lower" part consists of the resistor R28 in parallel with the resistance in the output

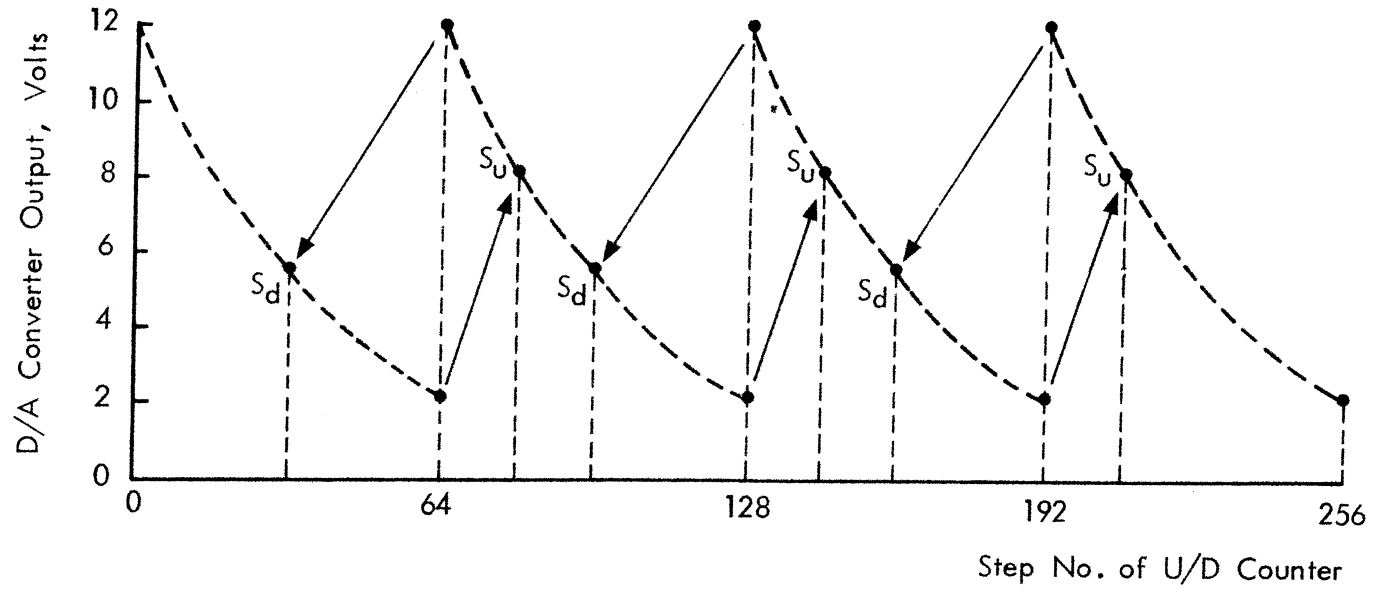


Fig. 2.2.5.6-4. Output Voltage of D/A Converter versus Step No. of U/D Counter.

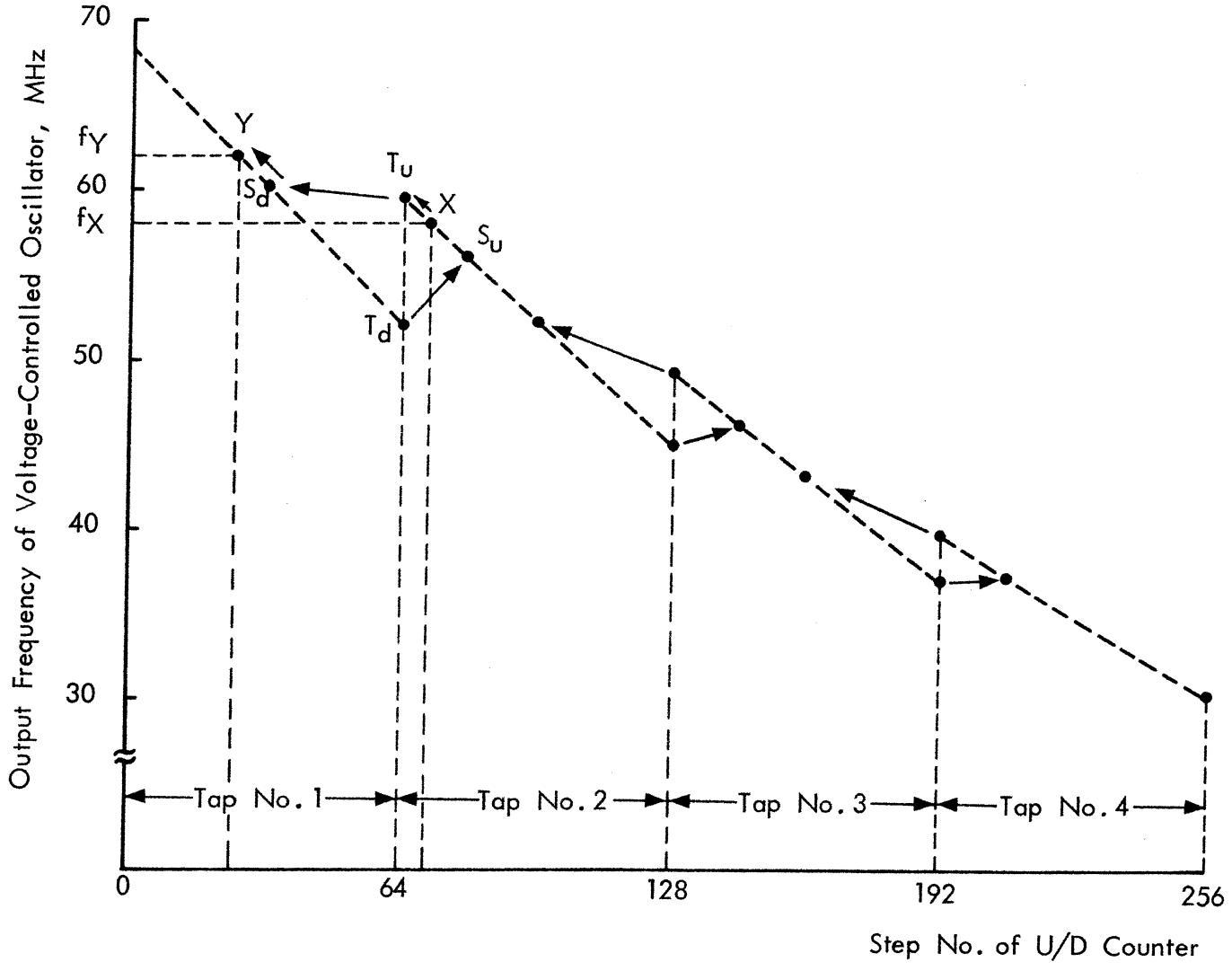


Fig. 2.2.5.6-5. Oscillator Frequency versus Step No. of U/D Counter.

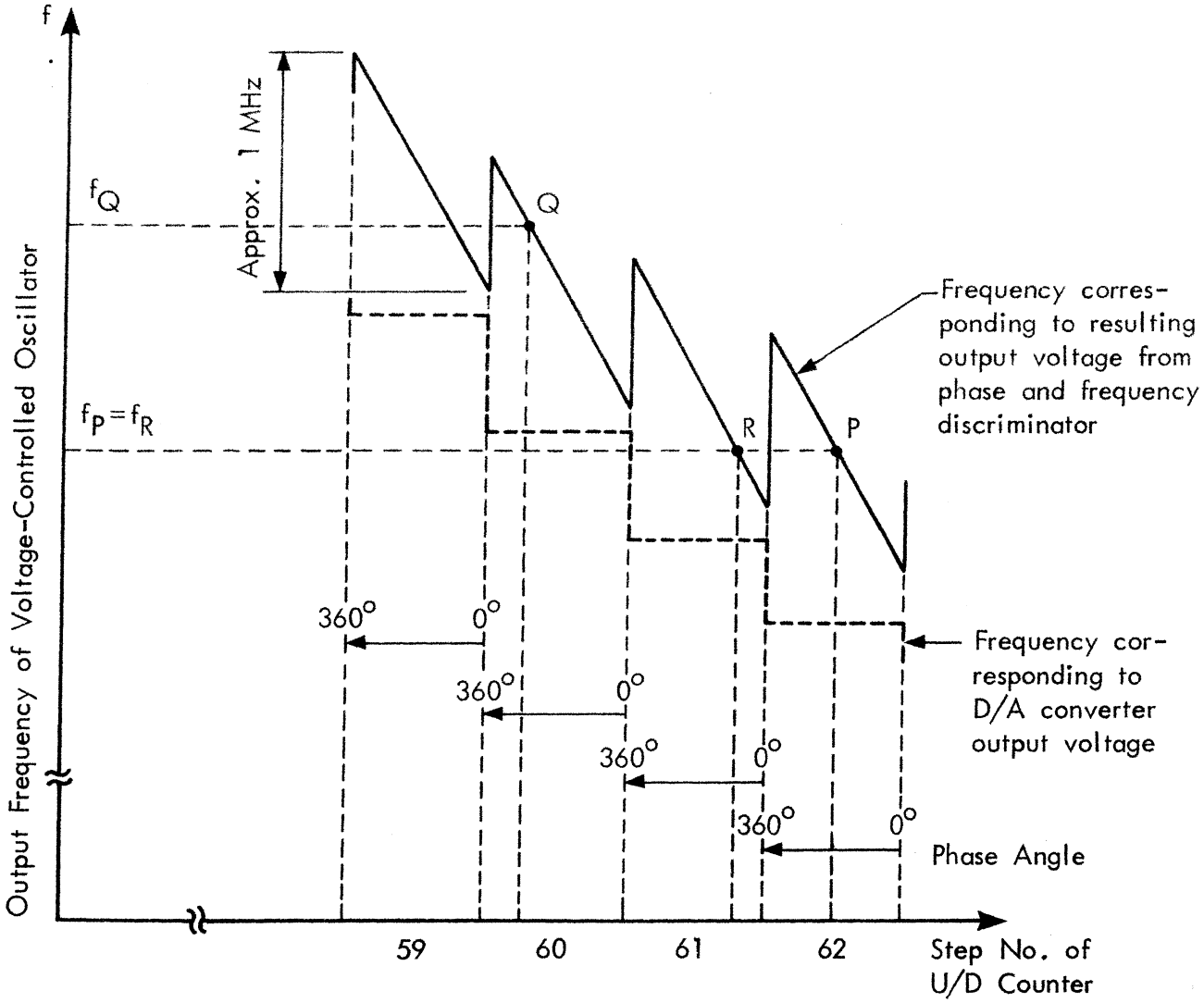


Fig. 2.2.5.6-6. Oscillator Frequency versus Phase Angle and Step No. of Up-Down Counter.

circuit of the D/A converter, in such a way that the loop gain is kept substantially constant. The combined signal from the phase and frequency discriminator is applied to the varactor diodes CR15 and CR16 in the oscillator tuning circuit through a low-pass filter which incorporates a notch filter for suppressing the reference-frequency signal. A graph representing the oscillator frequency as a function of the phase angle and the step number of the U/D counter is shown in Fig. 2.2.5.6-6. The principle of operation of the loop system is illustrated by the following examples:-

Example 1. - Change of frequency from f_P to f_Q (see Fig. 2.2.5.6-6):
The setting of the frequency division ratio is altered from that corresponding to fp to that corresponding to f_Q , and since $f_Q > f_P$ the output frequency from the frequency divider will be too low compared with the reference frequency. The U/D counter will then count down from step No.62 to step No.60 where the loop will be phase-locked.

Example 2. - Change of frequency from f_Q to f_R (see Fig. 2.2.5.6-6):
The setting of the frequency division ratio is altered from that corresponding to f_Q to that corresponding to f_R , and since $f_R < f_Q$ the output frequency from the frequency divider will be too high compared with the reference frequency. The U/D counter will then count up from step No.60 to step No.61 where the loop will be phase-locked. From the examples shown in Fig. 2.2.5.6-6 it will be seen that in this special case $f_R = f_P$, i.e. the same frequency

is obtained at different step numbers of the U/D counter. It should be noted that the frequency is decreased when the U/D counter counts up, and increased when the U/D counter counts down.

Example 3. - Change of frequency from f_X to f_Y (see Fig. 2.2.5.6-5):
The frequency f_X (at the point X on the curve) lies in the range covered by the step numbers 64 to 128 where tap No.2 has been selected. The frequency f_Y (at the point Y on the curve) lies in the range covered by the step numbers 0 to 64 so that it is necessary to change from tap No.2 to tap No.1 in order to arrive at this frequency. When the setting of the frequency division ratio is altered from that corresponding to f_X to that corresponding to f_Y the U/D counter will count down and cause the tap No.1 to be selected instead of tap No.2. After the tap on the oscillator tuning inductor has been changed the U/D counter should count further down and reach the step number corresponding to the frequency f_Y, but due to the time constant of the low-pass filter the voltage controlling the varactor diodes cannot change quickly enough and the oscillator frequency will then be too high, it may even be so high that, if no precautions were taken, the U/D counter would count up again and cause a change from tap No.1 to tap No.2 after which the U/D counter would count down again, etc. To overcome this problem the U/D counter is so arranged that every time the 7th bit is changed, i.e. when the inductor tap is changed, the U/D counter is automatically set to a condition which in the graphs Fig. 2.2.5.6-4 and Fig. 2.2.5.6-5 is represented by the point S_d when the counter counts down, and by the point S_u when the counter counts up. These points are placed so many steps away from the points T_d and T_u, where the change of inductor taps takes place, that the U/D counter is prevented from running into the unstable condition mentioned above. Therefore, when the tap No.1 has been selected instead of tap No.2, as mentioned above, and the U/D counter is set to the condition represented by the point S_d on the curve, the counter will first count up a few steps after which it will count down and reach the point Y for the frequency f_Y where the loop will be phase-locked.

When changing from one frequency to another the U/D counter will at the beginning count relatively fast in order to change the oscillator frequency in the direction of the desired frequency because the repetition rate of the output pulses from the discriminator is relatively high, but as the oscillator frequency approaches the desired frequency the U/D counter will count slower according to the lower repetition rate of the input pulses. If, for instance, the difference between the oscillator frequency and the desired frequency is about 10 kHz, the difference between the output frequency from the divider and the reference frequency is only a fraction of a Hz so that the time between two output pulses from the discriminator will be several seconds. However, in this case the output frequency from the divider will be within the capture range of the discriminator, which is about ±3 Hz from the 500-Hz reference frequency, and therefore the loop will be phase-locked. The time it takes for the synthesizer to reach the desired frequency when changing from a higher to a lower frequency is longer than the time it takes when changing from a lower to a higher frequency. This is illustrated by the following examples:-

Case A. - Change of oscillator frequency from 60 MHz to 30 MHz:
When the division ratio of the divider is altered from that corresponding to 60 MHz to that corresponding to 30 MHz, the output frequency from the divider will at the beginning be 1000 Hz. This is 500 Hz above the 500-Hz reference frequency.

Case B. - Change of oscillator frequency from 30 MHz to 60 MHz:
When the division ratio of the divider is altered from that corresponding to 30 MHz to that corresponding to 60 MHz, the output frequency from the divider will at the beginning be 250 Hz. This is 250 Hz below the 500-Hz reference frequency.

In case A the difference between the output frequency from the divider and the 500-Hz reference frequency at the beginning of the change is twice as high as in case B. Therefore, it will take nearly twice as long time for the synthesizer to reach the desired frequency in case A as it will in case B.

The output signal from the voltage-controlled oscillator is applied to a dual-channel output amplifier. The one output signal from this amplifier is applied to the prescaler in the 35.000-64.999 MHz variable-ratio frequency divider (Ref. Designation A3A7), while the other output signal is applied to a mixer in the s.s.b. modulator circuit (Ref. Designation A2A4). In order to prevent transmission as the voltage-controlled oscillator searches to achieve lock-up, the output amplifier is so arranged that the last-mentioned output channel is blocked when the loop is not phase-locked.

Voltage regulators are inserted in the power-supply leads to the D/A converter, and to the voltage-controlled oscillator and the output amplifier in order to provide the required high voltage stability. Two series regulators are used for the D/A converter, while a special series regulator with short-circuit protection is used for the voltage-controlled oscillator and the output amplifier.

2.2.5.7. 35.000-64.999 MHz Variable-Ratio Frequency Divider.
Reference Designation A3A7.

The plug-in module containing this divider is located in the frequency synthesizer drawer. The complete circuit diagram of the divider is located in the diagram section at the rear of this manual. As shown in the circuit diagram the plug-in module also contains filters for the +5-volt supply and the -5-volt supply, L1, C3, C5 and L2, C4, C6, four pull-down resistors, R8 to R11, fourteen pull-up resistors, R12 to R25, fourteen protecting zener diodes, CR8 to CR21, and an amplifier, ICB6, which is inserted in the input circuit to provide suitable clock pulses for driving a divide-by-two prescaler, ICA6, preceding the variable-ratio divider. The gate B6B operates as a linear amplifier while the following gate B6A provides a suitable amount of clipping. The input signal is obtained from the dual-channel amplifier in the 35-65 MHz loop circuit (Ref. Designation A3A6). The frequency of the input signal will lie within the range 35.000-64.999 MHz, i.e. the frequency of the output signal from the prescaler will lie within the range 17.5000-32.4995 MHz.

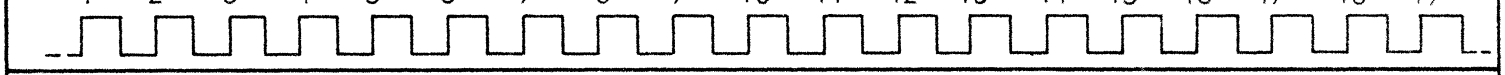
The variable-ratio frequency divider can be set to divide the frequency of the output signal from the prescaler by any integer between 35000 and 64999, the division ratio being determined by the positions of the binary-coded decade switches S2 ("0-9 kHz"), S3 ("0-90 kHz"), S4 ("0-900 kHz"), S5 ("0-9 MHz") and S6 ("0-20 MHz") on the frequency synthesizer front panel. This divider consists mainly of a synchronous decade divider, ICA1 to ICA5 and ICB1 to ICB5, which is controlled by the decade switch S2 (connections "A2", "B2", "C2" and "D2"), four cascaded asynchronous decade dividers, ICD2, ICE2, ICF1 and ICH1, which are controlled by the decade switches S3 (connections "A3", "B3", "C3" and "D3"), S4 (connections "A4", "B4", "C4" and "D4"), S5 (connections "A5", "B5", "C5" and "D5") and S6 (connections "A6", "B6", "C6" and "D6"), a decoder gate, ICE1, a strobe-input controlling flip-flop, ICD1, and fifteen adder gates, ICF2, ICF3, ICH2 and ICH3. Emitter-coupled logic (ECL) elements are used in the prescaler and the synchronous decade divider circuits, while transistor-transistor logic (TTL) elements are used in the asynchronous decade divider circuits. The logic levels for the two different logic systems are as follows:

For ECL elements: logic 0 ~ -1.5V and logic 1 ~ -0.7V
For TTL elements: logic 0 ~ 0V to +0.8V and logic 1 ~ +2.4V to +5V

Appropriate interface circuits are inserted in the divider circuit where logic elements of different families are interconnected, i.e. two ECL-to-TTL circuits, Q1, CR1, R2, R5, R26 and Q2, CR7, R4, R7, R27, and one TTL-to-ECL circuit, CR3 to CR6, R3, R6. It should be noted that the logic states 0 and 1 in the one logic system correspond to the respective logic states 0 and 1 in the other logic system so that the interface circuits may be ignored in the divider circuit diagram as regards the performance of logic functions.

The synchronous decade divider follows the 1-2-4-8 code. Its clock line is driven by the prescaler. Most of the time the synchronous decade divider operates as a divide-by-ten divider, i.e. for every ten input pulses it generates an output pulse which is applied to the input of the following asynchronous decade divider D2 via the interface circuit. But once during each division cycle of the complete 5-decade divider the synchronous decade divider counts some number from ten to nineteen, which is controlled by the decade switch, and then returns to count by ten again. It should be noted that initially the flip-flops in the synchronous decade divider are all in state Q=0 and $\bar{Q}$=1, and the flip-flop A1 is disabled by the flip-flop B1A, B1B and the gate B2B. The 8th input pulse in the count-by-ten sequence causes the flip-flop A2 to change state to Q=1 whereby the flip-flops A3 and A4 are disabled, their $\bar{Q}$ outputs remaining in state 1. On the receipt of the 9th input pulse the outputs of the flip-flop A2 will not change state because one $\bar{J}$ input as well as one $\bar{K}$ input are in state 1. The 10th input pulse causes the flip-flop A2 to change state to Q=0 again whereby the flip-flops A3 and A4 are enabled, thus restarting the counting sequence for the synchronous decade divider. The negative-going edge of the output pulse thus generated by the Q output of the flip-flop A2 triggers the input flip-flop in the asynchronous decade divider D2.

Table 2.2.5.7-1. Counting Sequence for Variable-Ratio Synchronous Decade Divider

Position of Decade Switch S2	'Divider State' preset by Decade Switch	Number of Input Pulses received after the condition of full has been reached in the four cascaded asynchronous decade dividers → 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19  'Divider State'																			Number of 'Divider States' at end of sequence
0	9	0	1	2	3	4	5	6	7	[9]	9	0									10
1	8	0	1	2	3	4	5	6	7	[8]	8	9	0								11
2	7	0	1	2	3	4	5	6	7	[7]	7	8	9	0							12
3	6	0	1	2	3	4	5	6	7	[6]	6	7	8	9	0						13
4	5	0	1	2	3	4	5	6	7	[5]	5	6	7	8	9	0					14
5	4	0	1	2	3	4	5	6	7	[4]	4	5	6	7	8	9	0				15
6	3	0	1	2	3	4	5	6	7	[3]	3	4	5	6	7	8	9	0			16
7	2	0	1	2	3	4	5	6	7	[2]	2	3	4	5	6	7	8	9	0		17
8	1	0	1	2	3	4	5	6	7	[1]	1	2	3	4	5	6	7	8	9	0	18
9	0	0	1	2	3	4	5	6	7	[0]	0	1	2	3	4	5	6	7	8	9	0	19

Most of the time the synchronous decade divider counts by ten, i.e. for every ten input pulses it generates an output pulse which is applied to the following asynchronous decade divider. But once during each division cycle of the complete 5-decade divider the synchronous decade divider counts some number from ten to nineteen, which is controlled by the decade switch, and then returns to counting by ten again.

When the condition of full is reached in the four cascaded asynchronous decade dividers, the flip-flop A2 is replaced by the flip-flop A1 so that the synchronous decade divider can be set to count in accordance with the position of the decade switch.

A pulse is applied to the strobe line so that the 'divider state' is modified according to the position of the decade switch. The gate B5B generates a short output pulse which is applied to the phase discriminator in the 35.000-64.999 MHz loop circuit.

The condition of full is reached in the complete 5-decade divider. The flip-flop A2 is again inserted in the circuit instead of the flip-flop A1. The synchronous decade divider will now count in accordance with the position of the decade switch and then return to counting by ten again (see the table: "Counting Sequence for 5-Decade Variable-Ratio Frequency Divider").

Each of the four cascaded asynchronous decade dividers, D2, E2, F1 and H1, follows the 1-2-4-8 code. Most of the time the decade dividers D2, E2 and F1 operate as divide-by-ten dividers. For every ten input pulses the decade divider generates an output pulse which is applied to the input of the following decade divider. But once during each division cycle of the complete 5-decade divider the decade divider counts some number from ten to nineteen, which is controlled by the decade switch, and then returns to count by ten again. The decade divider H1 does never count by ten, once during each division cycle of the complete 5-decade divider it counts some number, three, four, five or six, which is controlled by its decade switch and the adder circuit. The counting sequence for the variable-ratio synchronous decade divider is shown in Table 2.2.5.7-1, while the counting sequence for the 5-decade variable-ratio divider is shown in Table 2.2.5.7-2. In order to illustrate how the 'divider state' is modified according to the positions of the decade switches, an example is given in Table 2.2.5-7-3 for a division ratio of 26. It should be noted that in the actual divider the division ratio will never be lower than 35000.

When the condition of full is reached in the divider circuit comprising the four cascaded asynchronous decade dividers, i.e. the condition where these dividers are all in 'divider state' 9 (the 9999 content) and the outputs A and D are simultaneously in state 1, the output of the decoder gate E1 goes low, thus causing the flip-flop D1A,D1B to change state whereby the output of the gate D1A goes low while the output of the gate D1B goes high. The output of the gate D1A is connected to the strobe inputs of the four decade dividers D2, E2, F1 and H1 so that when this output goes low the 'divider state' is modified according to the positions of the decade switches S3, S4, S5 and S6. After this the output of the gate E1 goes high again without affecting the state of the flip-flop D1A,D1B. The output of the gate D1B is connected to the input of the gate B1A via the interface circuit so that when this output goes high the flip-flop B1A,B1B changes state. The flip-flop A2 in the synchronous decade divider is then disabled by the gate B3B while the flip-flop A1 is enabled by the gate B2B to operate when seven more input pulses have been counted by the synchronous decade divider. Thus, on the receipt of the next input pulse, i.e. the 8th input pulse after the full condition is reached in the four cascaded asynchronous decade dividers, the flip-flop A2 remains in state Q=0, the flip-flops A3 to A5 change state to $\bar{Q}$=1 while the flip-flop A1 changes state to Q=1 and $\bar{Q}$=0.

The output $\bar{Q}$=0 of the flip-flop A1 enables the appropriate decoder gates, B2A to B5A, to set the synchronous decade divider in accordance with the decade switch position. It also causes the flip-flops D1A,D1B and B1A,B1B to change state and the output of the gate B5B to go low, thus generating a negative-going output pulse which is applied to the phase discriminator in the 35.000-64.999 MHz loop circuit. The change of state of the flip-flop D1A, D1B enables the four cascaded asynchronous decade dividers to count in accordance with the decade switch positions. The output Q=1 of the flip-flop A1 disables the flip-flops A3 to A5 so that on the receipt of the following input pulse, i.e. the 9th input pulse after the full condition is reached in the four cascaded asynchronous decade dividers, the flip-flop A1, the $\bar{K}$ inputs of which are permanently at state 0, changes state to Q=0 and $\bar{Q}$=1 whereby the output of the gate B5B goes high, the flip-flops D1A,D1B and B1A,B1B obtain their original states and the flip-flops A2 to A5 are enables to count in accordance with the decade switch setting. It should be noted that the full condition has then been reached in the complete 5-decade divider, i.e. the 'divider state' corresponding to the 99999 content. On the receipt of the next input pulse the division cycle for the complete 5-decade divider is restarted.

At the start of the counting sequence for the 5-decade variable-ratio divider the synchronous decade divider will first count some number from zero to nine, which is controlled by its decade switch, and then return to count by ten until the condition of full (i.e. 9999 content) is reached in the four cascaded asynchronous decade dividers. Similarly, each of the decade dividers D2, E2 and F1 will first count some number from zero to nine, which is controlled by its decade switch, and then return to count by ten until the condition of full is reached in the four cascaded asynchronous decade dividers. The decade divider H1 will count some

Table 2.2.5.7-2. Counting Sequence for 5-Decade Variable-Ratio Frequency Divider.

Decade Switch	S6	S5	S4	S3	S2
Division-Ratio Digit	a	b	c	d	e
'Divider State' Digit preset by decade switch	9-a	9-b	9-c	9-d	9-e
m+1	9-a	9-b	9-c	9-d	10-e
⋮	⋮	⋮	⋮	⋮	⋮
9 9 9 7 9	9	9	9	7	9
9 9 9 8 0	9	9	9	8	0
9 9 9 8 1	9	9	9	8	1
9 9 9 8 2	9	9	9	8	2
9 9 9 8 3	9	9	9	8	3
9 9 9 8 4	9	9	9	8	4
9 9 9 8 5	9	9	9	8	5
9 9 9 8 6	9	9	9	8	6
9 9 9 8 7	9	9	9	8	7
9 9 9 8 8	9	9	9	8	8
9 9 9 8 9	9	9	9	8	9
9 9 9 9 0	9-a	9-b	9-c	9-d	0
9 9 9 9 1	9-a	9-b	9-c	9-d	1
9 9 9 9 2	9-a	9-b	9-c	9-d	2
9 9 9 9 3	9-a	9-b	9-c	9-d	3
9 9 9 9 4	9-a	9-b	9-c	9-d	4
9 9 9 9 5	9-a	9-b	9-c	9-d	5
9 9 9 9 6	9-a	9-b	9-c	9-d	6
9 9 9 9 7	9-a	9-b	9-c	9-d	7
9 9 9 9 8	9-a	9-b	9-c	9-d	9-e
9 9 9 9 9	9-a	9-b	9-c	9-d	9-e
m+1	9-a	9-b	9-c	9-d	10-e

Number of Input Pulses Counted from Preset Number to Full Condition

'Divider State'

Division Cycle

Division Ratio:
$N = ax10^4 + bx10^3 + cx10^2 + dx10 + e$

Preset Number:
$m = (9-a)x10^4 + (9-b)x10^3 + (9-c)x10^2 + (9-d)x10 + 9-e$

At the start of the counting sequence each decade divider counts some number from zero to nine, which is controlled by its decade switch (the preset 'divider state'), and then it counts by ten until the condition of full (i.e. the 9999 content) is reached in the four cascaded asynchronous decade dividers. The decade divider H1, however, only counts the number determined by the position of its decade switch.

The number of input pulses necessary to change the content m (the number preset on the divider) to the full condition (i.e. the 99999 content) in the complete 5-decade divider is equal to the division ratio, i.e.
$N = 99999 - m$

When the condition of full (i.e. the 9999 content) is reached in the four cascaded asynchronous decade dividers a pulse is applied to the strobe inputs of these dividers so that the 'divider state' is modified according to the setting of the decade switches S3, S4, S5 and S6.

A pulse is applied to the strobe line of the synchronous decade divider so that the 'divider state' is modified according to the setting of the decade switch S2, and a short output pulse is generated.

All decade dividers are set to count in accordance with the positions of the decade switches and on the receipt of the next input pulse the counting sequence is restarted.

Counting sequence repeated.

The 99999 content corresponding to full condition in the five-decade divider.

Table 2.2.5.7-3. Counting Sequence for 5-Decade Variable-Ratio Frequency Divider

Decade Switch						S6	S5	S4	S3	S2
Division-Ratio Digit						0	0	0	2	6
'Divider State' Digit preset by decade switch						9	9	9	7	3
Number of Input Pulses Counted from Preset Number to Full Condition	9	9	9	7	4	9	9	9	7	4
	9	9	9	7	5	9	9	9	7	5
	9	9	9	7	6	9	9	9	7	6
	9	9	9	7	7	9	9	9	7	7
	9	9	9	7	8	9	9	9	7	8
	9	9	9	7	9	9	9	9	7	9
	9	9	9	8	0	9	9	9	8	0
	9	9	9	8	1	9	9	9	8	1
	9	9	9	8	2	9	9	9	8	2
	9	9	9	8	3	9	9	9	8	3
	9	9	9	8	4	9	9	9	8	4
	9	9	9	8	5	9	9	9	8	5
	9	9	9	8	6	9	9	9	8	6
	9	9	9	8	7	9	9	9	8	7
	9	9	9	8	8	9	9	9	8	8
	9	9	9	8	9	9	9	9	8	9
	9	9	9	9	0	9	9	9	7	0
	9	9	9	9	1	9	9	9	7	1
	9	9	9	9	2	9	9	9	7	2
	9	9	9	9	3	9	9	9	7	3
	9	9	9	9	4	9	9	9	7	4
	9	9	9	9	5	9	9	9	7	5
	9	9	9	9	6	9	9	9	7	6
	9	9	9	9	7	9	9	9	7	7
	9	9	9	9	8	9	9	9	7	3
	9	9	9	9	9	9	9	9	7	3
	9	9	9	7	4	9	9	9	7	4

'Divider State'

Division Cycle (26 States)

Counting sequence repeated.

Example: a = 0, b = 0, c = 0, d = 2, e = 6

Division Ratio: $N = 0\times10^4+0\times10^3+0\times10^2+2\times10+6 = 20+6 = 26$

Preset Number: $m = (9-0)\times10^4+(9-0)\times10^3+(9-0)\times10^2+(9-2)\times10+9-6$

$= 9\times10^4+9\times10^3+9\times10^2+7\times10+3 = 99973\ (= 99999 - N)$

number, three, four, five or six, which is controlled by its decade switch and the adder circuit, once during a complete division cycle.

Once during each counting sequence the gate B5B produces an output pulse. As mentioned above, this output pulse is generated when the state of the $\bar{Q}$ output of the flip-flop A1 changes from 1 to 0 and then from 0 to 1 again. The total propagation delay time in this divider circuit is very short, because there are only seven stages in which delays can be introduced, i.e. the gates B6B and B6A, the flip-flops A6 and A1 and the gate B5B. This means that in the divider circuit used here the counter jitter is greatly reduced as compared with that which would occur in a corresponding ripple-through divider circuit containing approximately twenty stages.

The number of input pulses necessary to change the content m (the number preset on the divider) to the full condition in the complete 5-decade variable-ratio divider (i.e. the 99999 content) is equal to the division ratio N, i.e. $N=99999-m$. Thus, it is only necessary for the wiring of a decade switch to be arranged so that the nine's complement of each digit of the divisor is set in the corresponding decade. If, for example, the desired division ratio is $N=76027$, then the number to be preset on the divider is: $m=99999-N=99999-76027=23972$. The setting of the decade switches is also explained on the page containing the table for the counting sequence for the 5-decade variable-ratio frequency divider.

The principle of operation of the frequency synthesizer and the s.s.b. exciter is described in section 2.2.1. Block Diagram. It will be seen that the operating frequency of the 35.000-64.999 MHz variable-ratio frequency divider is 35000 kHz higher than the corresponding transmitting frequency, which is read on the dials for the decade switches on the synthesizer front panel. Consequently, the division ratio of the 5-decade variable-ratio divider must be 35000 higher than the number read on the dials for the decade switches. In order to obtain this, 35000 is added to the number corresponding to the binary information on the decade switches (i.e. the preset number m). 5000 is added to the preset number by displacing the dial for the decade switch S5 five steps from the position corresponding to the preset number. 30000 is added to the preset number by means of the adder circuit consisting of the gates F2, F3, H2 and H3. When the decade switch S5 is set in one of the positions "0", "1", "2", "3" or "4", 30000 is added to the preset number, but when the said switch is set in one of the positions "5", "6", "7", "8" or "9", 40000 is added to the preset number ("one is carried").

2.2.5.8. Output Gate-Off Circuit. Reference Designation A3A8.

The subassembly containing this circuit is located in the frequency synthesizer drawer and connected to the mother board wiring by means of p.c. card-to-card connectors. If an automatic fault localization device is required for the synthesizer, the subassembly containing the output gate-off circuit is replaced by a subassembly containing the a.f.l. device (Ref. Designation A3A10), the output gate-off circuit being incorporated in this device.

The output gate-off circuit consists mainly of a one-shot multivibrator, employing two transistors Q1 and Q2, followed by a buffer-amplifier transistor, Q3, and an indicator-lamp control transistor, Q4. Normally, the transistor Q1 is cut off and the transistor Q2 saturated. If a pulse having a positive-going or a negative-going edge is applied to the input, the multivibrator will change state, i.e. the transistor Q1 will be saturated and the transistor Q2 cut off. The multivibrator will remain in this state until the capacitor C2 has been discharged through the resistor R5 and the base voltage on the transistor Q2 has reached a value of approximately +0.5V, then the multivibrator will change state again, i.e. the transistor Q2 will be saturated and the transistor Q1 cut off. The pulse thus produced by the multivibrator will have a duration of approximately three seconds.

The input circuit of the one-shot multivibrator is connected to the output of the first stage of the up-down counter in the 35.000-64.999 MHz phase-locked loop module (Ref. Designation A3A6) so that when the up-down counter changes state, i.e. when an out-of-lock condition exists, the one-shot multivibrator will produce a three-second output pulse. This pulse is amplified by the transistor Q3 and applied to the gated output amplifier, A3A6IC8, in the 35.000-64.999 MHz phase-locked loop plug-in module whereby the transmitting signal is blocked for approximately three seconds, thus allowing sufficient time for the loop to achieve lock-up. The output pulse from the buffer amplifier is also applied to the indicator-lamp control transistor Q4, which switches on the indicator lamp DS2 ("test") on the s.s.b. exciter front panel so that this lamp will light when the loop is not phase-locked.

2.2.5.9. 1.5-MHz Signal-Level Control Circuit. Reference Designation A3A9.

The subassembly containing this circuit is located in the frequency synthesizer drawer and connected to the mother board by means of soldered terminals and wires. The purpose of the circuit is to provide means for adjusting the maximum level of the output signal from the s.s.b. exciter to the desired values for transmitting frequencies in the medium-frequency range and the intermediate-frequency range, respectively. For the high-frequency range the maximum obtainable signal level is desired. Since the balanced modulator in the s.s.b. exciter has a linear characteristic the desired output-signal levels of the s.s.b. exciter can be obtained by controlling the level of the 1.5-MHz input signal to the modulator.

As shown in the circuit diagram, the 1.5-MHz output signal from the standard-frequency oscillator circuit (Ref. Designation A3A3) is applied to the control circuit through a coaxial cable connected to the socket J1, while the 1.5-MHz output signal from the control circuit is applied to the balanced modulator (Ref. Designation A2A4) in the s.s.b. exciter through a coaxial cable connected to the socket J2. When the frequency synthesizer is adjusted for a transmitting frequency in the medium-frequency range, the relay K1 is energized whereby the adjustable load resistor R1 is inserted across the terminals for the 1.5-MHz signal. Similarly, when the synthesizer is adjusted for a transmitting frequency in the intermediate-frequency range, the relay K2 is energized whereby the adjustable load resistor R2 is inserted across the terminals for the 1.5-MHz signal. The resistors R1 and R2 are pre-adjusted at the factory to provide the proper signal levels for transmitting frequencies in the medium-frequency range and the intermediate-frequency range, respectively. The relays K1 and K2 are fed from the output of the 20-volt rectifier in the rectifier-circuit module (Ref. Designation A3A1). It should be noted that this supply of 20V will not be available for the relays if the regulator-circuit module (Ref. Designation A3A2) is withdrawn, because the 20-volt rectifier obtains its ground connection from the regulator-circuit module, see paragraph 2.2.5.1.

2.2.5.10. Automatic Fault Localization Device. Reference Designation A3A10.

The automatic fault-localization (a.f.l.) device is supplied on special request. The subassembly containing this device is designed to be located in the frequency synthesizer drawer and connected to the mother board wiring by means of p.c. card-to-card connectors. If an a.f.l. device is supplied, it replaces the subassembly containing the output gate-off circuit (Ref. Designation A3A8), the output gate-off circuit being incorporated in the a.f.l. device subassembly. The complete a.f.l. circuit can be divided into fifteen individual circuits, i.e. fourteen signal-sensing circuits and a fault-localizing circuit.

In order to check the operation of the frequency synthesizer the fourteen signal-sensing circuits are connected to appropriate circuits contained in the plug-in modules. If the circuit being checked operates properly the signal-sensing circuit in question provides an output signal of logic level 1, but in case of faulty operation the signal-sensing circuit provides an output signal of logic level 0. The outputs of the signal-sensing circuits are connected to the inputs of the fault-localizing circuit through the test points designated "A", "B", "C", "D", "E", "F", "H", "K", "L", "M", "N", "P", "R" and "S" in the circuit diagram. Some of the signal-sensing circuits are contained in the plug-in modules. The signal sources to be checked are:-

Test Point:	Signal source:	Ref. Designation of the plug-in module:
"A"	500-Hz reference output from frequency standard	A3A3
"B"	500-Hz output from 33.4991-33.5000 MHz variable-ratio divider	A3A5
"C"	35.000-64.999 MHz output from phase-locked loop	A3A6
"D"	500-Hz output from 35.000-64.999 MHz variable-ratio divider	A3A7
"E"	30-MHz output from frequency standard	A3A3
"F"	Phase-control output from 35.000-64.999 MHz phase-locked loop	A3A6
"H"	Phase-control output from 33.4991-33.5000 MHz phase-locked loop	A3A4
"K"	1.5-MHz output from frequency standard	A3A3
"L"	33.4991-33.5000 MHz output from phase-locked loop	A3A4
"M"	17.4955-17.5000 MHz output from phase-locked loop	A3A4
"N"	+17-volt regulated output from voltage-regulator circuits	A3A2
"P"	+12-volt regulated output from voltage-regulator circuits	A3A2
"R"	-5-volt regulated output from voltage-regulator circuits	A3A2
"S"	Unregulated outputs and -12-volt regulated output from rectifiers	A3A1

The fault-localizing circuit has seven outputs, one for each plug-in module. To each output is connected a transistor in the emitter circuit of which is inserted an indicator lamp. The output signals from the signal-sensing circuits are applied simultaneously to the fault-localizing circuit. If the frequency synthesizer operates properly the outputs from the signal-sensing circuits will all be at logic level 1, and none of the indicator lamps mentioned above will light. If the circuit in a plug-in module fails to operate properly the output from the signal-sensing circuit concerned will be at logic level 0, and the fault-localizing circuit will cause the indicator lamp for the plug-in module in question to light, thus indicating in which plug-in module the faulty circuit is localized. Similarly, if faults occur in two or more plug-in modules simultaneously, the indicator lamps for all the faulty modules will be lighted. The indicator lamps for the plug-in modules are located on top of the subassembly containing the a.f.l. device so that they are visible when the frequency synthesizer drawer is withdrawn. An extra indicator lamp, which is located on the front panel and designated "test", is lighted when a fault occurs in a plug-in module, but in order to find out where the fault is localized the frequency synthesizer drawer must be withdrawn so that the indicator lamps for the plug-in modules are visible.

The principle of operation for the a.f.l. device is shown in the simplified circuit diagram Fig. 2.2.5.10-1. The outputs from the circuits to be checked in a plug-in module are sensed by the signal-sensing circuits Nos. 1-4, while the inputs to the circuits are sensed by the signal-sensing circuits Nos. 5-7, these inputs being provided by circuits contained in other plug-in modules. The outputs from the signal-sensing circuits Nos. 1-4 are fed to the gate F,

and if the circuits being checked in the plug-in module are operating properly all these outputs will be high (at logic level 1) so that the output of the gate F will be low (at logic level 0). The output from the gate F is fed to one input of the gate C while the outputs from the signal-sensing circuits Nos. 5-7 are fed to the other inputs of the gate C, and if the circuits are operating properly these outputs will be high. The output of the gate C will be high because the output of the gate F is low. If one of the circuits in the plug-in module to which the signal-sensing circuits Nos. 1-4 are connected fails to operate, the output of the signal-sensing circuit concerned goes low whereby the output of the gate F will go high, and provided that the outputs of the signal-sensing circuits Nos. 5-7 are all high the output of the gate C will go low, thus causing the indicator lamp in the emitter circuit of the output transistor to be lighted. If more than one circuit in the plug-in module fail to operate the indicator lamp will still be lighted. However, if one of the outputs from the signal-sensing circuits Nos. 5-7 is low the output of the gate C will remain high and the indicator lamp will not be lighted, but in this case the fault, which must have occurred in one of the plug-in modules employing the signal-sensing circuits Nos. 5-7, will be localized by means of the fault-localizing gates and indicator lamp for the plug-in module in question.

The signal-sensing circuit No. 1 is used for sensing the output signal from a phase discriminator. The circuit operates as a one-shot multivibrator. If a positive-going or a negative-going pulse edge appears at the input the one-shot multivibrator circuit will be triggered and its output will go low for approximately three seconds and then fall back to the stable state, the time being determined by the RC time constant of the circuit.

The signal-sensing circuit No. 2 is used for sensing a 500-Hz output signal from an ECL circuit. The signal-sensing circuit employs an ECL flip-flop which is triggered by the 500-Hz (repetition rate) signal. The output signal from the flip-flop is amplified and detected. The signal from the detector is fed to an output amplifier. The output of this amplifier is high as long as the 500-Hz input signal is present, but if the 500-Hz signal fails the output of the amplifier goes low.

The signal-sensing circuit No. 3 is used for sensing a high-frequency signal. The input circuit employs a pair of ECL gates connected as a linear amplifier and detector. The output signal from the detector is amplified by two transistors. The output of the circuit is high when the proper input signal is present, but if the input signal fails the output goes low.

The signal-sensing circuit No. 4 operates in a way similar to that of circuit No. 2. In this case the input signal is obtained from a TTL circuit, and a TTL flip-flop is employed in the input circuit.

The signal-sensing circuit No. 5 operates as a positive d.c. level detector. If the voltage obtained from the voltage divider Ra,Rb, which is inserted across the supply voltage, falls below a pre-determined value the output of the circuit goes low.

The signal-sensing circuit No. 6 operates as a negative d.c. level detector. The voltage divider Rc,Rd is inserted between the positive 5-volt supply lead and the negative voltage supply lead. If the voltage between the tap on the voltage divider and ground (chassis) is correct the output of the signal-sensing circuit is high, but if the negative supply voltage fails the output of the circuit goes low.

The signal-sensing circuit No. 7 is used for sensing a high-frequency signal. The input signal is amplified and detected. The signal from the detector is applied to an output amplifier. The output of the circuit is high when the proper input signal is present, but if the input signal fails the output goes low.

The operation of the frequency synthesizer is checked continuously by means of its a.f.l. device, while the push-button designated "test" on the front panel of the s.s.b. exciter must be pressed in order to check the operation of the exciter.

It should be noted that the indicator lamp on the front panel of the frequency synthesizer will

light and indicate "faulty operation" immediately after the setting of the frequency synthesizer has been altered if the frequency is altered so much that the loop cannot remain phase-locked. The indicator lamp will then be lighted for approximately three seconds, during which time proper phase-lock should be established.

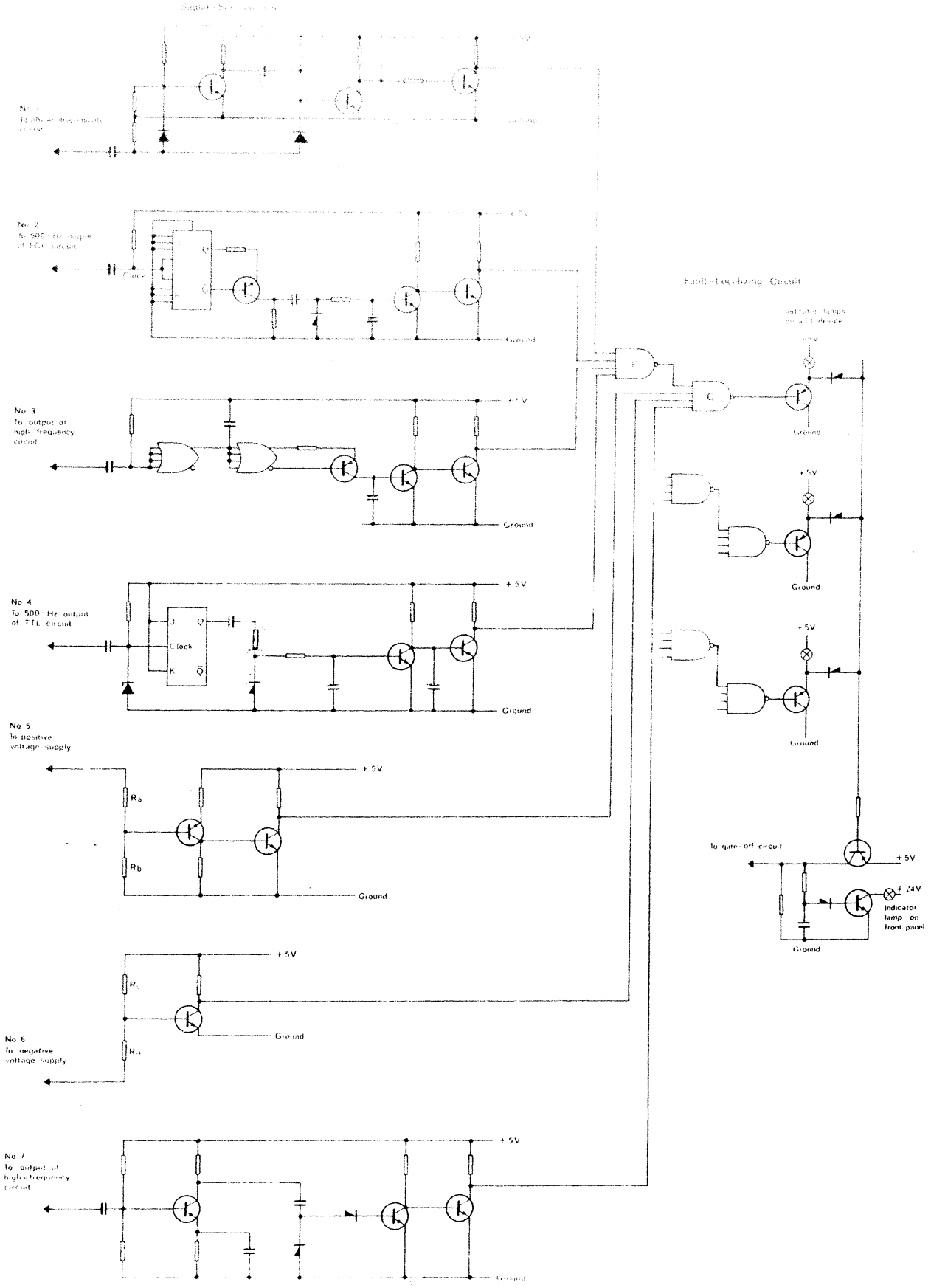


Fig. 2.2.5.10-1. Principle of Operation of Automatic Fault Localization Device.

2.2.6. Power Amplifier Circuit. Reference Designations A4, A4A1 and A4A2.

The panel-and-chassis assembly (drawer) for the power amplifier also contains a wide-band driver amplifier (Subassembly Ref. Designation A4A1) preceding the power amplifier, and three power supplies (Subassembly Ref. Designation A4A2) providing power for the wide-band amplifier and grid bias for the power amplifier valve. A complete circuit diagram is located in the diagram section of this manual.

The wide-band driver amplifier is a linear amplifier designed to operate in the range 400 kHz to 30 MHz. It employs one transistor, A4A1Q1. The output signal from the exciter is applied to the input of the wide-band driver amplifier through a coaxial cable. The output signal from the wide-band amplifier is fed to the control grid of the power amplifier valve through a matching filter circuit comprising the inductors L1 and L2, which are pre-adjusted for maximum output at 25 MHz. It may be necessary to re-adjust these inductors if the power amplifier valve is replaced by a new valve.

A stabilized collector-supply voltage of +27V for the transistor Q1 is provided by the rectifier CR7 and the voltage regulator circuit employing the transistors A4A2Q1-to-Q5, while a stabilized bias supply of 3.0V to 4.5V for the base circuit is provided by the rectifier CR2 and the voltage regulator circuit employing the integrated circuit A4A2IC1 and the transistors A4A2Q6-and-Q7. These voltages are pre-adjusted to the correct values by means of the potentiometers A4A2R7-and-R16. A negative grid bias of approximately -32V to -35V for the power amplifier valve is provided by the rectifier CR4 and the voltage regulator circuit employing the transistors A4A2Q8-to-Q12. The negative grid bias for the power amplifier valve is pre-adjusted to the correct value by means of the potentiometer A4A2R24 (typical grid bias -34V). The above-mentioned potentiometers in the voltage regulator circuits are accessible for adjustment when the cover plate for the voltage regulator underneath the chassis is removed.

The power amplifier stage employs a radial beam power tetrode type 4CX1500B (8660), which is operated as a linear Class AB amplifier. Forced-air cooling is provided by a blower, B1, which is started by means of the relay K5 when the push-button switch designated "start" on the main power-supply front panel is pressed, and simultaneously the full heater voltage is applied to the valve. The anode and screen-grid voltages are provided by rectifiers located in the main power supply assembly (Ref. Designation A1), see paragraph 2.2.3. where instructions for pre-adjusting the screen-grid voltage to the correct value are given. The thermistor RT1, which is mounted on the anode connector of the power amplifier valve, is connected to the overload-control circuit in the main power supply assembly. In the case of overload the indicator lamp DS1 on the front panel is lighted.

The anode voltage is applied to the power amplifier valve V1 through the r.f. chokes L5, L6 or L7, the proper r.f. choke being selected by means of the relay K3 which is controlled by the decade switches on the frequency synthesizer front panel. When the synthesizer is adjusted for a frequency within the range 0.4-1 MHz all the r.f. chokes L5, L6 and L7 are series-connected, while for frequencies within the range 1-7 MHz the r.f. chokes L6 and L7 are series-connected, and for frequencies within the range 7-30 MHz only the r.f. choke L7 is used. The said decade switches also control the relay K4 which selects the proper antenna matching network, i.e. the medium-frequency antenna matching network (Ref. Designation A6) for frequencies within the range 400 kHz to 535 kHz, and the intermediate and high-frequency antenna matching network (Ref. Designation A5) for frequencies within the range 1.6 MHz to 27.5 MHz.

The meter M1 is switched by means of S2 to indicate the anode voltage, the control-grid voltage, the screen-grid voltage, the anode current and the screen-grid current of the power amplifier valve. See also Section 3.- Meters and Indicators.

The meter M2, which has zero-point indication at about one fifth of the full scale length, is used as a tuning and loading indicator. The r.f. voltage detectors comprising the diodes CR1 and CR2 are connected to the control-grid circuit and the anode circuit of the power amplifier valve to sample the respective r.f. voltages. When the switch S1, which is located on

the front panel near the meter M2 and designated "tune/power", is set in position "tune" the detector outputs are combined to feed the meter. When the correct ratio of anode signal voltage to grid signal voltage exists, the detector outputs are balanced and cause no meter deflection. As the signal level on the control grid remains constant the meter will dip when the power-amplifier tank circuit, i.e. the antenna tuning network, is tuned to resonance. When the degree of coupling to the antenna is increased, the dip-point reading on the meter at resonance will move to the right on the scale and, similarly, when the degree of coupling to the antenna is decreased the corresponding dip-point reading will move to the left on the scale. The transmitter is continuously keyed by means of the relay K6 when the switch S1 is in position "tune", and the A2H-emission oscillator is switched on. When the switch is set to position "read power" the transmitter is continuously keyed with the A2H-emission oscillator switched on as mentioned above, but the meter is disconnected from the anode circuit so that only the detected signal from the control-grid circuit is applied to the meter. The meter deflection then corresponds to the output power of the transmitter if the power amplifier stage is correctly tuned and loaded. The tuning and loading indicator circuit is pre-adjusted for proper operation on the medium-frequency range as well as on the intermediate and high-frequency ranges by means of the adjustable resistors R16,R23,R19 and R20, the appropriate resistors being selected by the relays K1 and K2. These relays are controlled by the decade switches on the frequency synthesizer front panel. When the switch S1 is set to the mid-position, "0", the meter is connected to the grid circuit as well as the anode circuit, but the transmitter is not keyed.

2.2.7. Intermediate-Frequency and High-Frequency Antenna Matching Network. Reference Designation A5.

The i.f. and h.f. antenna matching network is contained in a panel-and-chassis assembly located above the power amplifier. The basic configuration of the antenna matching network is a π-L filter circuit. The complete circuit diagram is located in the diagram section at the rear of this manual. The variable capacitors C1 and C3 are controlled from the front panel by knobs designated "tune" and "antenna coupling", respectively. The ganged 12-position inductance and capacitance selector switch S1 is controlled from the front panel by a knob designated "band selector". On the front panel are also located an antenna ammeter, M1, designated "antenna current", and an indicator lamp, DS1, designated "HF/IF".

The antenna matching network is automatically switched into circuit by means of the frequency-range selector relays in the power amplifier assembly (Ref. Designation A4) and the antenna switching relays in the cabinet rack when the frequency synthesizer is adjusted for a frequency within the i.f. and h.f. ranges. The indicator lamp DS1 is controlled by the synthesizer decade switches so that it lights when a frequency within the i.f. and h.f. ranges is selected. The selector switch S1 is combined with the interlock switch S2 which is connected to the input of the function control circuit (Ref. Designation A2A8). When the interlock switch S2 is closed the function control circuit inhibits the keying circuit of the transmitter. By this means the signal voltage is removed from the selector switches in the antenna matching network while switching over from one position to another.

The tuning of the antenna circuit depends entirely on the characteristics of the actual antenna at the operating frequency. In order to obtain correct tuning and proper loading of the power amplifier at all frequencies within the bands which can be selected by the ganged "band selector" switch S1, the various connections from the switch sections to the appropriate inductor taps and capacitors must be pre-set immediately after the transmitter has been installed so that it can be operated in connection with the actual antenna, see section 5 of this manual.

2.2.8. Medium-Frequency Antenna Matching Network. Reference Designation A6.

The m.f. antenna matching network is contained in a panel-and-chassis assembly located above the i.f. and h.f. antenna matching network. The basic configuration of the antenna matching network is an L filter circuit. The complete circuit diagram is located in the diagram section at the rear of this manual. The variometer L1 is controlled from the front panel by a knob designated "fine tune". The 9-position inductance selector switches S1 and S2 are controlled from the front panel by knobs designated "coarse tune" and "antenna coupling", respectively. On the front panel are also located an antenna ammeter, M1, designated "antenna current", and an indicator lamp, DS1, designated "MF".

The antenna matching network is automatically switched into circuit by means of the frequency-range selector relays in the power amplifier assembly (Ref. Designation A4) and the antenna switching relays in the cabinet rack when the frequency synthesizer is adjusted for a frequency within the m.f. range. The indicator lamp DS1 is controlles by the synthesizer decade switches so that it lights when a frequency within the m.f. range is selected. The function of the interlock switch S3 is similar to that of the interlock switch A5S2 in the i.f. and h.f. antenna matching network described above.

The tuning of the antenna circuit depends entirely on the characteristics of the actual antenna at the operating frequency. In order to obtain correct tuning and proper loading of the power amplifier at all frequencies, the various connections from the "coarse tune" switch S1 to the appropriate taps on the variometer must be pre-set immediately after the transmitter has been installed so that it can be operated in connection with the actual antenna, see section 5 of this manual.

SECTION 3. - METERS AND INDICATORS.

3.1. Meters.

On the front panel of the power amplifier panel-and-chassis assembly are located the following meters:-

The volt and milliammeter A4M1, scale: 0-100, and its five-position meter switch A4S2. The voltages and currents which can be measured are:-

Switch position "V_{g1}", scale range 0-100V:	The control-grid voltage (negative bias) for the power amplifier valve.
Switch position "V_a", scale range 0-10000V:	The anode-supply voltage for the power amplifier valve.
Switch position "I_a", scale range 0-1000 mA:	The anode current of the power amplifier valve.
Switch position "I_{g2}", scale range 0-100 mA:	The screen-grid current (negative) of the power amplifier valve.
Switch position "V_{g2}", scale range 0-1000V:	The screen-grid supply voltage for the power amplifier valve.

Typical Test Data:-

It should be realized that the following readings are not exaxt values for every operating condition. They were taken with the transmitter adjusted for A3J operation ("test" condition) and full power, i.e. 375 W p.e.p. for the m.f. and i.f. ranges and 1000 W p.e.p. for the h.f. range.

Negative grid bias:	V_{g1} = 32V to 36V, typical value 34V
Anode-supply voltage:	V_a = 3000V
Anode-current, m.f. range:	I_a = approx. 480 mA
i.f. range:	I_a = approx. 425 mA
h.f. range:	I_a = approx. 680 mA
Screen-grid current:	I_{g2} = 10 mA to 20 mA
Screen-grid supply voltage:	V_{g2} = 220V to 250V, typical value 230V

The meter A4M2 which has zero-point indication at about one fifth of the full scale length. The zero point is designated " $\longrightarrow 0 \longleftarrow$ " and "tune for dip", and the scale to the right of the zero point is designated "power": "1/16, 1/6, 1/3, 1/2, 3/4, 1". When the switch designated "tune/power" on the front panel is set to position "tune" the meter functions as a tuning and loading indicator. When the said switch is set to position "read power" the meter functions as a power meter. Operating instructions for the meter are given in Section 6 of this manual. After the correct tuning and loading adjustments have been obtained and the power-control knob has been adjusted for the required output power, the "tune/power" switch A4S1 should be set to its mid-position "0".

An antenna ammeter is provided on the front panel of each antenna matching network panel-and-chassis assembly, the meter A6M1 for the m.f. range and the meter A5M1 for the i.f. and h.f. ranges.

3.2. Indicator Lamps.

On the front panel of the main power supply assembly are located the following indicator lamps:-

The indicator lamp A1DS1, designated "stand by", which is lighted when the transmitter is switched to stand-by condition.

The indicator lamp A1DS2, designated "on", which is lighted when the anode and screen-grid power supplies are switched on.

On the front panel of the s.s.b. exciter panel-and-chassis assembly is located an indicator lamp A2DS1, designated "test". This lamp is used only if the s.s.b. exciter is equipped with an automatic fault localization device. The a.f.l. device is switched on by means of the push-button switch to the left of the lamp. If a fault occurs in the s.s.b. exciter the indicator lamp A2DS1 will light when the push-button is pressed, but in order to find out where the fault is localized the s.s.b. exciter drawer must be withdrawn so that the indicator lamps for the plug-in modules are visible. These indicator lamps are located on top of the subassembly containing the a.f.l. device and are designated "A2", "A3", "A4", "A5" and "A7" corresponding to the reference designations of the plug-in modules being checked (Ref. Desig. Prefix A2). The indicator lamps for the faulty modules will light when the said push-button switch is pressed.

On the front panel of the frequency synthesizer panel-and-chassis assembly are located the following indicator lamps:-

The indicator lamp A3DS1, designated "distress", which is lighted when the frequency synthesizer is set on 500 kHz or 2182 kHz.

The indicator lamp A3DS2, designated "test", which is lighted when the 35.000-64.999 MHz loop is not phase-locked. If the frequency synthesizer is equipped with an automatic fault localization device, this indicator lamp will also light in the case of faulty operation of the synthesizer, but in order to find out where the fault is localized the synthesizer drawer must be withdrawn so that the indicator lamps for the plug-in modules are visible. These indicator lamps are located on top of the subassembly containing the a.f.l. device and are designated "A1", "A2", "A3", "A4", "A5", "A6" and "A7" corresponding to the reference designations of the plug-in modules being checked (Ref. Design. Prefix A3). The indicator lamps for the faulty modules will light. The a.f.l. device for the frequency synthesizer is continuously connected into circuit.

It should be noted that the indicator lamp A3DS2 will light and indicate "faulty operation" immediately after the setting of the frequency synthesizer has been altered if the frequency has been altered so much that the loop cannot remain phase-locked. The indicator lamp will then be lighted for approximately three seconds, during which time proper phase-lock should be established.

On the front panel of the power amplifier panel-and-chassis assembly is located an indicator lamp A4DS1, designated "overload", which is lighted when the power amplifier valve is overloaded.

On the front panel of the panel-and-chassis assembly for the intermediate and high-frequency antenna matching network is located an indicator lamp A5DS1, designated "IF/HF", which is lighted when the i.f. and h.f. antenna matching network is in use.

On the front panel of the panel-and-chassis assembly for the medium-frequency antenna matching network is located an indicator lamp A6DS1, designated "MF", which is lighted when the m.f. antenna matching network is in use.

SECTION 4. - INSTRUCTIONS FOR INSTALLATION.

The mounting dimensions of the transmitter are shown in the outline dimensional drawing located in the diagram section at the rear of this manual. The transmitter should be so located that there is sufficient clearance at each side for free circulation of air and for connecting the antenna and ground. A minimum clearance of 110 mm should be left behind the transmitter to afford access for the air tube and the air inlet filter. Sufficient space should also be allowed in front of the transmitter for the panel-and-chassis assemblies to be withdrawn and for manipulation of the control knobs and reading of meters, etc. While mounting the cabinet rack all the panel-and-chassis assemblies should be removed from the cabinet rack, see section 2.1, and the side plates may also be removed temporarily. The external cables are passed into the cabinet rack through an entering hole in the rear plate. The panel-and-chassis assemblies should not be placed in the cabinet rack again until this is in position and properly bolted to the base, and the external cables are connected to the terminal board on the rear plate.

The external wiring should be made in accordance with the installation wiring diagram. The antenna lead-in should be provided with a grounding switch so that the transmitter may be disconnected and the antenna grounded when not in use. The antenna lead-in and the ground connection for the transmitter should be made in accordance with the drawing showing the recommended arrangement of antenna and ground connections, which drawing is located in the diagram section at the rear of this manual together with the outline dimensional drawings of the transmitter, the handset, and the handset socket. It is very important that the transmitter is effectively grounded to the ship's main metal structure outside the radio cabin at the antenna lead-in insulator. The terminal on the lead-through insulator on top of the transmitter is intended for connecting an antenna conductor consisting of a 6-mm dia. copper tube to the transmitter. The ground terminal on the rear plate of the cabinet rack is intended for connecting a ground conductor consisting of a 0.4 mm thick and 200 mm wide copper strip to the transmitter. The conductor cross-sectional area of the power-supply cables should be of sufficient size to offer a voltage drop of not more than 2 %.

The transmitter is designed to operate into the normal main antenna used aboard ship for medium frequencies, i.e. for the m.f. range the antenna should have an effective resistance of from 1.9 Ω to 3.6 Ω and an apparent capacitance of from 750pF to 300pF. Normally, this main antenna is also used for the i.f. and h.f. ranges. One of the most simple and easily installed types of antenna, which is suitable for operation on all frequencies within the frequency ranges covered by the transmitter, is the inverted "L" antenna. This consists of a horizontal flat-top section with a single-wire lead-in connected to one end. The antenna length should be considered as the combined length of the flat-top and lead-in sections. Where possible, avoid the vicinity of half-wavelength antennas or multiples thereof, since it may be difficult to obtain proper loading on the frequencies concerned.

When the installation is completed, the panel-and-chassis assemblies should be placed in the cabinet rack again and all the plugs inserted in their respective sockets. The equipment should be tested and the antenna matching networks pre-adjusted as described in the following section of this manual before the equipment is put into service.

SECTION 5. - PRE-ADJUSTMENTS OF ANTENNA MATCHING NETWORKS.

5.1. Precaution and Special Instructions.

When the equipment has been installed, the antenna matching networks should be adjusted for correct tuning and proper loading of the power amplifier stage with the actual antenna connected to the transmitter. These adjustments should be made with the ship's antennas placed in their normal positions, but if the ship is alongside quay, see that no cranes, derricks, etc. are near the antenna since these may interfere with the adjustments.

The capacitors and inductors of the antenna matching network are accessible for adjustment when the panel-and-chassis assembly containing the network is withdrawn to its stop position. For some adjustments it may be necessary to remove the entire panel-and-chassis assembly from the cabinet rack, see paragraph 2.1 in this instruction manual. After each adjustment has been made, the panel-and-chassis assembly should be pushed into position in the cabinet rack and the transmitter operated to check the adjustment. It may be necessary to try several adjustments before the correct tuning and loading are arrived at.

The adjustment procedures for the antenna matching networks are outlined below. When the adjustments for all the required frequencies and frequency bands are completed, the settings of the control knobs should be recorded in a "Tuning Table" together with the corresponding meter readings, and a copy left on the radio station for the operator.

5.2. Pre-adjustment of I.F. and H.F. Antenna Matching Network.

The i.f. and h.f. antenna matching network is designed to operate into the normal main antenna used aboard ship for medium frequencies. A shorter antenna may be used, but it must have sufficient length to provide a capacitance of at least 150pF at 1.6 MHz. The main antenna usually consists of an end-fed long-wire antenna (inverted "L" antenna) which has a natural frequency considerably higher than the highest operating frequency in the medium-frequency range, i.e. the antenna length is much smaller than a quarter wavelength. When such an antenna is used for the i.f. and h.f. ranges, resonance is obtained whenever the total antenna length approximates a multiple of a quarter wavelength for the frequency involved. At frequencies on one side of a resonance point, the reactance will be inductive; on the other side of the resonance, it will be capacitive. Typical resistance and reactance curves for a long-wire antenna are shown in Fig. 5.2-1. The antenna length in terms of wavelength, i.e. the ratio of the antenna length to the wavelength, can be calculated by means of the following approximate formula, which allows for end effects:

Antenna length in terms of wavelength
= 0.0034 x (total length of antenna in metres) x (operating frequency in MHz).

The total length of the antenna should be considered as the combined length of the flat-top and lead-in sections. Since ship antennas are installed near numerous metal elements of large dimensions such as funnels, masts, rigging, etc., which influence the antenna impedance characteristic, it is difficult to make exact calculations of the antenna resistance and reactance. The formula above and the curves in Fig. 5.2-1 should be used only as a rough guide, e.g. if it is desired to find out for a given frequency whether the antenna is operated near a resonance point, or whether the reactance is positive or negative. The impedance characteristic of a "T" antenna, or a special ship "mast" antenna, may differ greatly from that of a normal end-fed single-wire antenna.

The i.f. and h.f. antenna matching network is described in paragraph 2.2.7 and the complete circuit diagram is located in the diagram section at the rear of this manual.

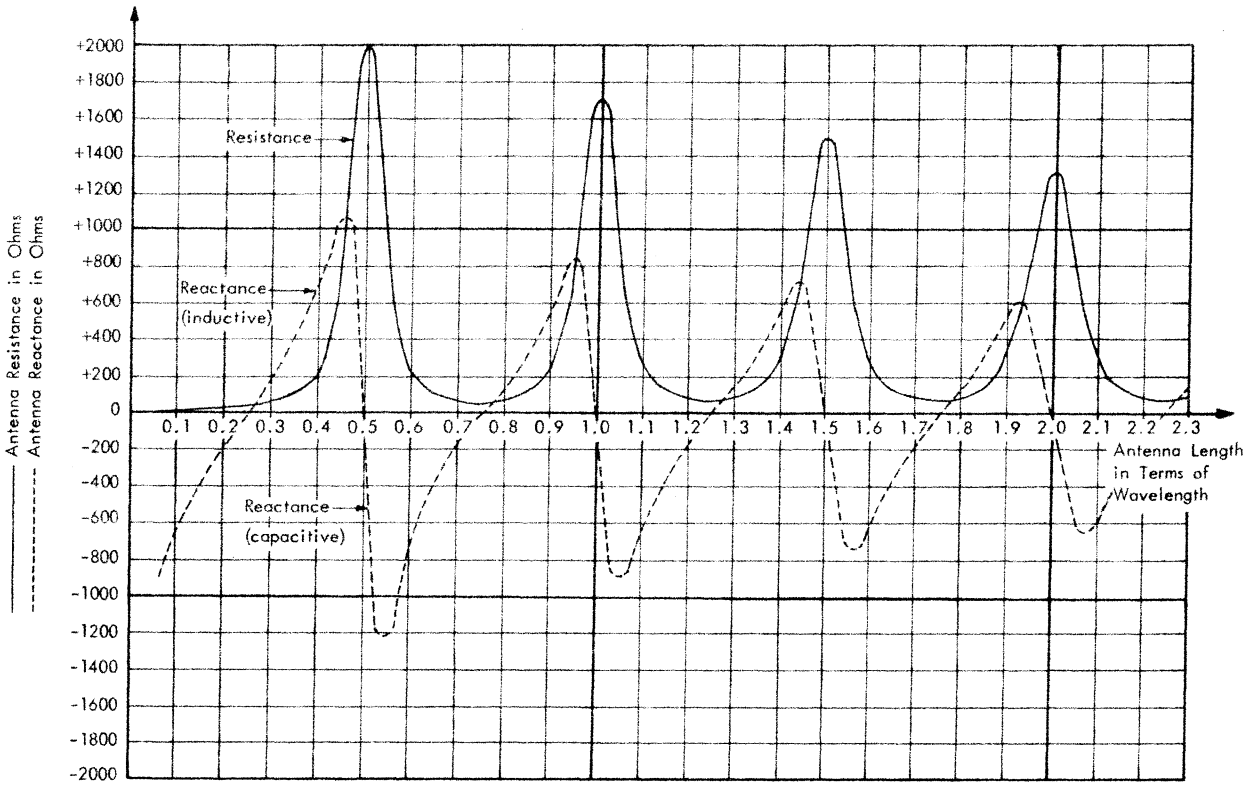


Fig. 5.2-1. Resistance and Reactance versus Antenna Length in Terms of Wavelength for an End-Fed Long-Wire Antenna. Typical Curves.

5.2.1. 1.6 MHz to 3.8 MHz Range.

Normally a π-L network is used for this frequency range. It comprises the variable input capacitor C1, the fixed input capacitor C2, the tapped inductor L1, the variable output capacitor C3, and the tapped series inductor L4. A fixed capacitor, C4, C5, C6 or C8, may be inserted across the variable output capacitor C3. If a short antenna is used it may be necessary to insert a suitable part of the tapped inductor L5 across the output capacitor at the lower operating frequencies.

The band selector switch section S1-d selects the proper taps on the inductor L1 for tuning the circuit to the five different bands within the i.f. range, while fine tuning to the transmitting frequency in question is made by adjusting the variable capacitor C1.

The degree of coupling to the antenna is adjusted by means of the variable capacitor C3. The required fixed capacitor, C4, C5, C6 or C8, is selected by the switch section S1-g, or if a parallel inductance is required this switch section selects the proper tap on the inductor L5. The switch section S1-f selects the proper tap on the antenna loading inductor L4.

In many cases the factory-adjusted "normal" network will give satisfactory matching to the antenna at the higher frequencies within the range, so that it is only necessary to readjust the taps on the inductor L1 at the lower operating frequencies. The natural frequency of the antenna will usually lie between 2.4 MHz and 3.0 MHz, and at frequencies lower than the natural frequency the antenna reactance will be capacitive so that a suitable series inductance may be required. Therefore, it is often necessary also to readjust the taps on the series inductor L4 at the lower operating frequencies. At the higher operating frequencies it is us-

ually necessary to insert a suitable fixed capacitor (100pF to 400pF) across the variable capacitor C3.

If the antenna is short, e.g. a rod antenna, it may be necessary to use parallel inductance at all operating frequencies and series inductance at the lower operating frequencies.

When the adjustments are completed and the transmitter is operated with the power control adjusted for full power, the anode current of the power amplifier valve should be approximately 450mA.

5.2.2. 4 MHz to 12 MHz Range.

The network used for this frequency range is similar to that described above, but the inductor L1 is replaced by the inductor L2.

The band selector switch section S1-d selects the proper taps on the inductor L2 for tuning the circuit to the four different bands, i.e. the 4-MHz band, the 6-MHz band, the 8-MHz band, and the 12-MHz band, while fine tuning to the transmitting frequency in question is made by adjusting the variable capacitor C1.

The degree of coupling to the antenna is adjusted by means of the variable capacitor C3. The degree of coupling may be decreased by means of a fixed capacitor, C4, C5, C6 or C8, which can be switched into circuit by the switch section S1-g. For the 4-MHz, 6-MHz and 8-MHz bands a series inductance may be required. The loading inductor L4 is inserted in series with the antenna by means of the tap selecting switch S1-f.

After the degree of coupling to the antenna has been adjusted, the tuning must be checked and the tap on the inductor L2 readjusted, if required.

If the antenna is short it may be necessary to reduce the series inductance (L4) in order to increase the degree of coupling to the antenna on the 4-MHz band. In some cases a parallel inductance may be required on the 4-MHz and 6-MHz bands. If the tap position on the series inductor L4 has been readjusted or the parallel capacitance altered, the tuning must be checked again and the tap on the inductor L2 readjusted, if required. When the series inductance (L4) is reduced it is often necessary to readjust the coupling capacitance by means of a suitable parallel capacitor.

On the 6-MHz band the antenna resistance may be very high (near half-wave resonance). In this case the series inductance L4 should be omitted (short-circuited) and proper matching be obtained by selecting the appropriate tap on the inductor L2 and adjusting the variable capacitors C1 and C3.

5.2.3. 16 MHz to 27.5 MHz Range.

The network used for this frequency range is a π-network similar to that described above. The inductor L2 is replaced by the inductor L3 and the series inductor L4 is omitted (short-circuited). Fine-adjustment of the inductor L3 is obtained by means of a slug which is controlled by the knob of the variable capacitor C1. On the 22-MHz and 25-MHz bands the capacitor C1 is disconnected so that only the stray capacitance forms the input capacitance of the π-circuit.

The band selector switch S1-d selects the proper taps on the inductor L3 for tuning the circuit to the three different bands, i.e. the 16-MHz band, the 22-MHz band, and the 25-MHz band, while fine tuning to the transmitting frequency in question is made by adjusting the control knob for the capacitor C1.

The degree of coupling to the antenna is adjusted by means of the variable capacitor C3. It

should be noticed that on the higher frequency bands, especially the 22-MHz and 25-MHz bands, the coarse tuning of the circuit is obtained by adjusting the variable coupling capacitor C3, after which the fine tuning is obtained by adjusting the control knob for the tuning capacitor C1 (slug tuning).

The following procedure should be used to tune the transmitter on the 22-MHz and 25-MHz bands:-

Set the tuning control in the middle of its scale range (about 45 scale divisions).

Adjust the coupling control for resonance in the antenna circuit, i.e. for dip on the tuning indicator. Resonance will probably be obtained with the coupling control adjusted in a position at the higher end of its scale range (80-90 scale divisions).

Fine-adjust the tuning control for resonance in the circuit, i.e. for dip on the tuning indicator.

Repeat these tuning and coupling adjustments and find the position of the antenna coupling control where the dip-point reading occurs at zero on the meter scale. Finally, readjust the tuning control.

When the power control is adjusted for full power the anode current of the power amplifier valve should be between 700 mA and 800 mA (for all frequencies in the h.f. range).

5.3. Pre-adjustment of M.F. Antenna Matching Network.

The m.f. antenna matching network is described in paragraph 2.2.8 and the complete circuit diagram is located in the diagram section at the rear of this manual. The basic configuration of the matching network is an L filter circuit. In the m.f. range practical ship antennas are always capacitive and have low resistance (high Q).

The adjusting procedure for a given frequency is as follows, see also section 6.- Operating Instructions:-

Set the type-of-emission selector on "A1".

Set the frequency selector knobs (decade switches) on the frequency synthesizer front panel to the positions for the required frequency.

Set the "coarse tune" switch and the "coupling" switch on the front panel of the m.f. antenna matching network assembly in provisional positions, e.g. their mid-positions.

Start the transmitter. The indicator lamp designated "on" will light when the power amplifier valve is warmed up.

Turn the power control to zero, anti-clockwise. Set the switch designated "tune/power" on the power amplifier front panel to position "read power" and advance the power control until the meter designated "tune/power" (tuning indicator) indicates approximately "1/6" on the "power scale".

Set the "tune/power" switch to position "tune" and adjust the variometer knob, designated "fine tune", for resonance in the antenna circuit, i.e. for dip on the tuning indicator, designated "tune/power".

Find the position of the "coarse tune" switch where resonance is obtained with the variometer knob adjusted in the middle of its scale range.

Adjust the antenna coupling control S2 in accordance with the dip-point reading. If the dip-

point reading occurs to the right of the zero point on the tuning indicator, the degree of coupling to the antenna should be decreased, and if the dip-point reading occurs to the left of the zero point, the degree of coupling to the antenna should be increased, i.e. the arrow on that side of the zero point on the meter scale where the dip-point reading occurs indicates the direction in which the antenna coupling control should be turned in order to move the dip-point reading towards the zero point.

Adjust the antenna coupling control so that the dip-point reading occurs at zero or as close to zero as possible on the meter scale and readjust the variometer knob for resonance. When the power control is adjusted for full power the anode current of the power amplifier valve should be between 500 mA and 600 mA.

It is recommended that the setting of the coupling (the choice of tap on L4) should first be made at the highest operating frequency (512 kHz) with the antenna coupling control set in a position near the higher end of its scale range. Then the required lower degree of coupling at the lower operating frequency can be obtained by turning the antenna coupling control to the appropriate position within the lower range of the scale.

The taps for the other operating frequencies on the antenna variometer should be adjusted in a similar way to that described above, and it should be checked that the proper coupling to the antenna at all the operating frequencies can be obtained by adjusting the antenna coupling control.

It should be noticed that when the frequency synthesizer is set on 500 kHz the s.s.b. exciter is unconditionally adjusted for A2H operation by means of the function control circuit.

SECTION 6. - OPERATING INSTRUCTIONS.

6.1. Starting the Equipment.

While the ship is at sea the temperature-controlled oven for the standard-frequency oscillator should be continuously switched on and the filament of the power amplifier valve be switched on at reduced voltage. This is done by means of the switch designated "stand by" on the power supply panel. When the button of this switch is pressed the pilot lamp designated "stand by" will light indicating that the "stand by" power is on.

Before starting the transmitter, see that the button designated "simplex" on the s.s.b. exciter panel is pressed. If duplex operation is required, the button designated "duplex" should not be pressed until the transmitter is properly adjusted and the desired telephone connection established.

In order to switch on all the supply voltages in the transmitter, press the switch button designated "start" on the power supply panel and when the cathode of the power amplifier valve is warmed up to its correct temperature the pilot lamp designated "on" will light indicating that the supply voltages are on. If the "stand by" power has been switched on for more than two minutes before the button designated "start" is pressed, only one minute is required for the cathode of the power amplifier valve to warm up. If the transmitter is started directly by means of the button designated "start", about three minutes are required for the cathode of the power amplifier valve to warm up.

Set the type-of-emission selector on the s.s.b. exciter panel on the required type of emission: "A1", "A2H", "F1", "A3H", "A3A" or "A3J".

Adjust the "power control" knob on the s.s.b. exciter panel for a relatively low output power.

Set the frequency selector knobs (decade switches) on the synthesizer panel to the positions for the required frequency and tune the antenna circuit as described in section 6.3 for the medium-frequency range, or section 6.4 for the intermediate- and high-frequency range. See also the "Tuning Table" made on installation.

It should be noted that the frequency read on the synthesizer is the transmitting carrier frequency.

6.2. Stopping the Equipment.

When the ship is at sea, press the switch button designated "stand by" in order to keep the equipment ready for use, see section 6.1. In order to switch off the transmitter completely, switch off the external main switch for the equipment.

6.3. Tuning the Transmitter in the Medium-Frequency Range.

Set the type-of-emission selector on the required type of emission: A1 or A2H.

Set the frequency selector knobs (decade switches) on the synthesizer panel to the positions for the required frequency.

Set the antenna tuning switch, the antenna tuning control and the antenna coupling control on the front panel of the medium-frequency tuning unit in accordance with the settings given in the "Tuning Table".

Turn the power control to zero, anti-clockwise. Set the switch designated "tune/power" on the power amplifier panel to position "read power" and advance the power control until the meter designated "tune/power" indicates approximately "1/6" on the "power scale".

After this, set the switch designated "tune/power" to position "tune" and adjust the tuning control on the panel of the medium-frequency tuning unit for dip on the meter designated "tune/

power" (tuning indicator). If the dip-point reading occurs to the right of the zero point on the tuning indicator, the degree of coupling to the antenna should be decreased, and if the dip-point reading occurs to the left of the zero-point, the degree of coupling to the antenna should be increased, i.e. the arrow on that side of the zero point on the meter scale where the dip-point reading occurs indicates the direction in which the antenna coupling control should be turned in order to move the dip-point reading towards the zero point. Re-adjust the antenna coupling control in accordance with the dip-point reading.

Repeat these tuning and loading adjustments and find the position of the antenna coupling control where the dip-point reading occurs at zero or as close to zero as possible on the meter scale.

Set the switch marked "tune/power" to position "read power" and adjust the power control for the required output power read on the "power" scale.

Finally, before working the transmitter, set the switch marked "tune/power" in position "0".

6.4. Tuning the Transmitter in the Intermediate- and High-Frequency Ranges.

Set the type-of-emission selector on the required type of emission (if f.s.k. operation is required the transmitter should first be tuned with the button for A3J emission pressed. The button for F1 emission should not be pressed until the tuning and loading adjustments are completed).

Set the frequency selector knobs (decade switches) on the synthesizer panel to the positions for the required frequency.

Set the antenna tuning switch, the antenna tuning control and the antenna coupling control on the front panel of the intermediate- and high-frequency tuning unit in accordance with the settings given in the "Tuning Table".

Turn the power control to zero, anti-clockwise. Set the switch marked "tune/power" on the power amplifier panel to position "read power" and advance the power control until the meter marked "tune/power" indicates approximately "1/6" on the "power scale".

After this, set the switch marked "tune/power" to position "tune" and adjust the tuning control on the panel of the intermediate- and high-frequency tuning unit for dip on the meter marked "tune/power" (tuning indicator). If the dip-point reading occurs to the right of the zero point on the tuning indicator, the degree of coupling to the antenna should be decreased, and if the dip-point reading occurs to the left of the zero point, the degree of coupling to the antenna should be increased, i.e. the arrow on that side of the zero point on the meter scale where the dip-point reading occurs indicates the direction in which the antenna coupling control should be turned in order to move the dip-point reading towards the zero point. Re-adjust the antenna coupling control in accordance with the dip-point reading.

Repeat these tuning and loading adjustments and find the position of the antenna coupling control where the dip-point reading occurs at zero on the meter scale.

Set the switch marked "tune/power" to position "read power" and adjust the power control for the required output power read on the "power" scale.

Finally, before working the transmitter, set the switch marked "tune/power" in position "0".

When the transmitter is operated on A3H, A3A or A3J and the desired telephone connection is established, the button marked "duplex" may be pressed whereby the transmitter is continuously keyed for duplex operation.

Note. Never change over from one operating frequency to another while working duplex or F1. While changing frequency, switch over to simplex operation or A1 operation.

SECTION 7. - MAINTENANCE.

7.1. General.

It is recommended that the user should become familiar with the contents of SECTION 2. - DESCRIPTION before attempting the adjustment or replacement of component parts of the equipment.

7.2. Checking the Standard-Frequency Oscillator.

The method of checking the frequency of the standard-frequency oscillator by making comparisons with broadcast standard-frequency signals requires the use of a receiver covering the 5-, 10-, 15- or 20-MHz bands. The output from the "x500 kHz" socket, J10, on top of the frequency synthesizer should be loosely coupled to the antenna circuit of the receiver as shown below in Fig.7.2-1. The socket J10 is accessible when the synthesizer drawer is pulled out to its stop position. A list of radio stations transmitting standard frequencies is given in the ITU Publication "List of Radiodetermination and Special Service Stations".

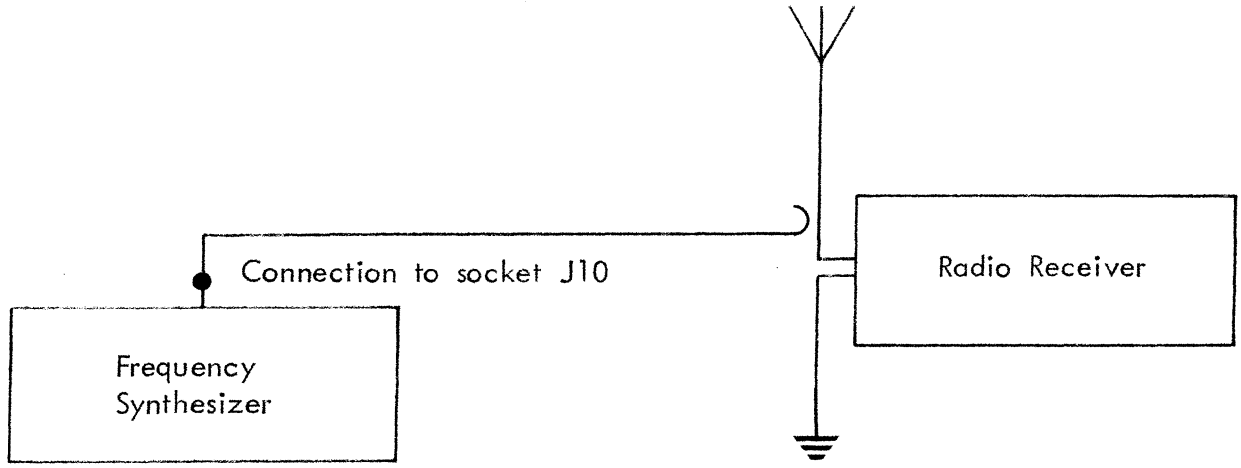


Fig.7.2-1. Diagram of Connections for Checking the Standard-Frequency Oscillator.

After allowing a warming-up period of at least 20 minutes for the frequency synthesizer and the receiver, proceed as follows:-

1) Select the standard-frequency broadcast station from which the reception of signals is best and tune it in with the receiver beat-frequency oscillator switched on and adjusted for a beat-note of approximately 1000 Hz.

2) Place the wire from the "x500 kHz" output, J10, on the frequency synthesizer near the antenna input terminal of the receiver in order to provide a suitable degree of coupling between the synthesizer and the receiver.

3) The audio-frequency output signal from the receiver should then be a beat-note of approximately 1000 Hz varying at a rate corresponding to the difference between the standard frequency of the radio station and the nearest harmonic of 500 kHz (the "x500 kHz" signal from the synthesizer). For best results the signal from the radio station and the signal from the synthesizer output should be about the same strength. Rearrange the coupling wire if necessary.

) Wait for the transmission period during which the modulation is absent. Then adjust the frequency of the standard-frequency oscillator by means of the potentiometer R1 in the

voltage-control circuit of the oscillator until its harmonic is in zero beat with the frequency of the standard-frequency radio station. The potentiometer R1 is located on the mother board in the synthesizer panel-and-chassis assembly and is accessible for adjustment by a screwdriver through a hole in the top cover plate, designated "R1 STANDARD CALIBRATE". The exact setting is found by observing the slow rise and fall in intensity (not frequency) of the beat note as the harmonic comes close to zero beat, and adjusting to where the pulsation disappears or occurs at a very slow rate It is advisable not to try to set the standard-frequency oscillator during the periods when the standard-frequency transmission is tone-modulated, since it is difficult to tell whether the harmonic is being adjusted to zero beat with the carrier or with one of the side bands.

SECTION 8. - ALIGNMENT.

8.1. General.

This frequency synthesizer equipment should maintain its correct factory adjustment over a reasonably long period of time. No one but an authorized and competent service man equipped with proper test facilities should be permitted to align the equipment. It is emphasized that realignment must not be attempted until all other causes for subnormal performance have been investigated. In order to gain access to the appropriate trimmer capacitors, iron-dust cores, potentiometers, etc. the plug-in module to be tested must be mounted on an extension plug-in board in the synthesizer panel-and-chassis assembly with the slide-out cover removed as illustrated below.

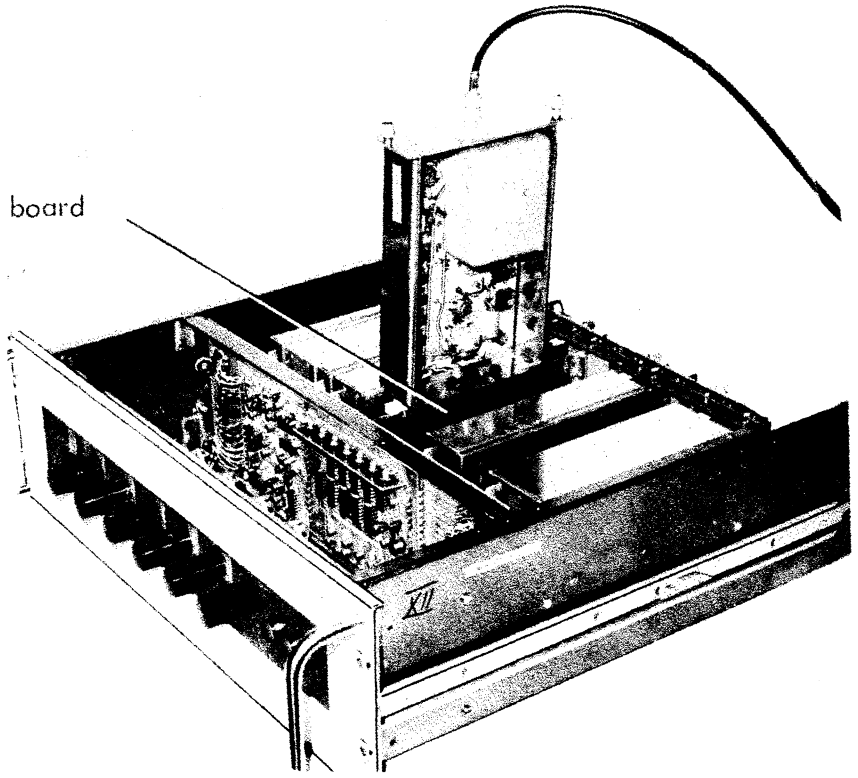


Fig. 8.1-1. Plug-in Module mounted on an Extension Plug-in Board.

While aligning a plug-in module, all the other plug-in modules of the frequency synthesizer must remain inserted in their proper positions in the panel-and-chassis assembly.

The test equipment must include a test oscilloscope for checking the amplitude and waveform of the signals and an electronic counter for measuring the frequency. These instruments must meet or exceed the following specifications:

Test Oscilloscope. Bandwidth, d.c. to 80 MHz; minimum deflection factor 5 mV/division; accuracy within 10%; test probe, -20 dB (high impedance). Tektronix Type 454 Oscilloscope recommended.

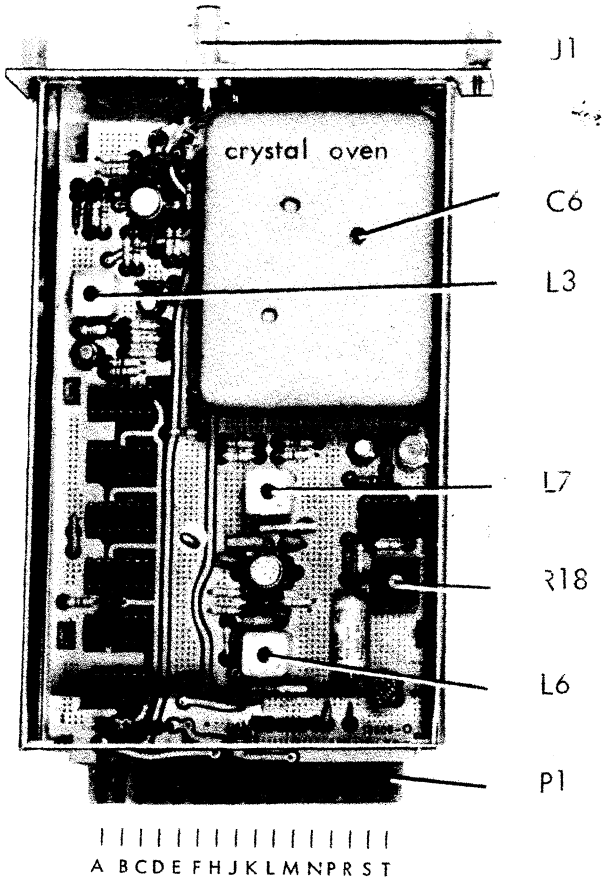
Electronic Counter. Max. frequency 80 MHz; accuracy 1×10^{-7}; minimum sensitivity 25 mV r.m.s. A lower sensitivity may be sufficient if the test oscilloscope has an output socket for the vertical amplifier to which the electronic counter can be connected.

The alignment procedure for the plug-in modules having the reference designations A3 and A4 are outlined on the following pages. It should be noted that the "typical readings" are only given as a rough guide.

Plug-in Module for Frequency Standard.

Reference Designation, Transmitter Equipment: S1250A3A3
Receiver Equipment: M1250SYNA3

PC boards Nos. 18800 and 18809.



Alignment Procedure:

After allowing a warming up time of at least 20 minutes, proceed as follows:-

1. Connect a 50-Ω load to J1 and adjust L3 for max. output signal across this load.

   Output frequency: 1.5 MHz
   Typical output level: 600 to 700 mVpp

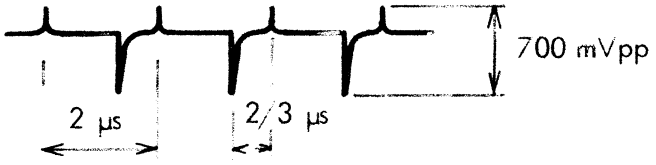
2. (For transmitter plug-in modules only). Adjust L7 and L6 for max. output signal from P1-D.

   Output frequency: 30 MHz
   Typical output level: 300 to 500 mVpp

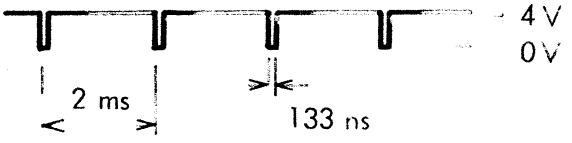
3. Adjust R18 for correct temperature, 75° C, on the surface of the oven chamber. The temperature should be measured by means of an electronic thermometer, the temperature-sensing probe being applied to the oven chamber surface through the hole for trimmer C6 in the heat-insulating cover.

4. Adjust the potentiometer R1 on the mother board in the synthesizer for a voltage of 3 V dc at P1-C. Adjust C6 for correct frequency of the output signal from J1, i.e. exactly 1500000.0 Hz.

Waveform of signal at P1-A:



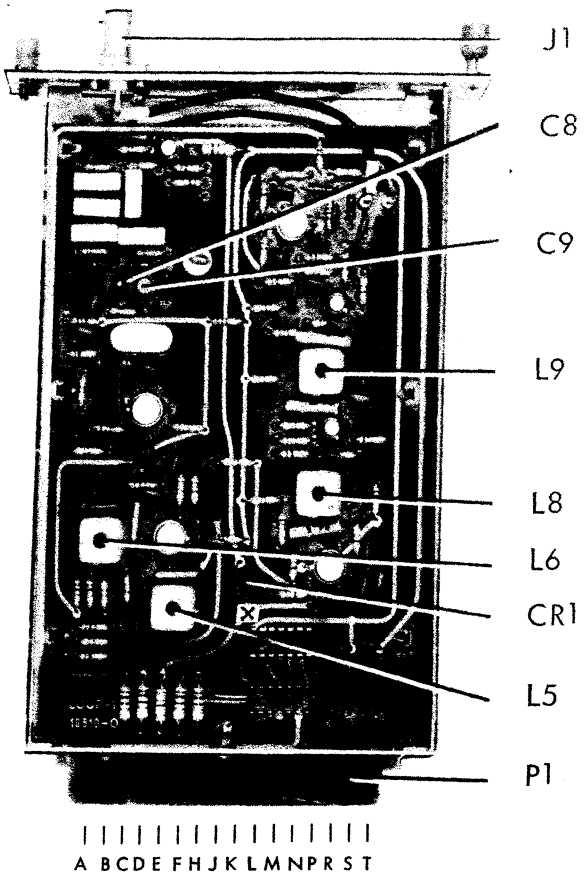
Waveform of signal at P1-H:



Plug-in Module for 33.4991-33.5000 MHz Phase-Locked Loop.

Reference Designation, Transmitter Equipment: S1250A3A4

PC board No. 18810.



Alignment Procedure:

1. Adjust L6 and L5 for max. output signal from P1-D.

   Output frequency: 17.5 MHz
   Typical output level: 500 to 700 mVpp

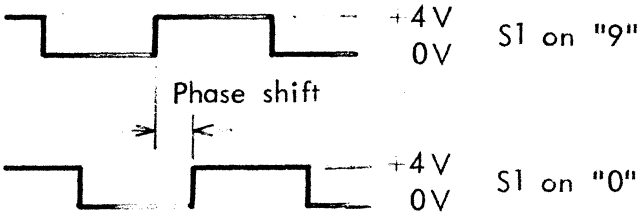
   (Be aware that the circuit by mistake can be adjusted for 14 MHz or 21 MHz).

2. Connect a 50-Ω load to J1 and adjust L8 and L9 for max. output signal across this load.

   Output frequency: 33.5 MHz
   Typical output level: 350 to 500 mVpp

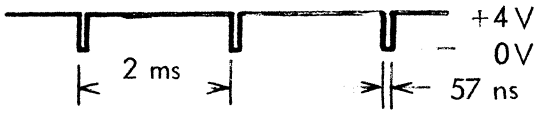
3. Adjust C8 for min. phase shift when changing the setting of the decade switch S1 on the front panel from "0" to "9", the phase shift being measured on the signal at test point "X" near CR1.

Waveform of signal at point "X":



Waveform of signal at P1-H:

Waveform of signal at P1-F:

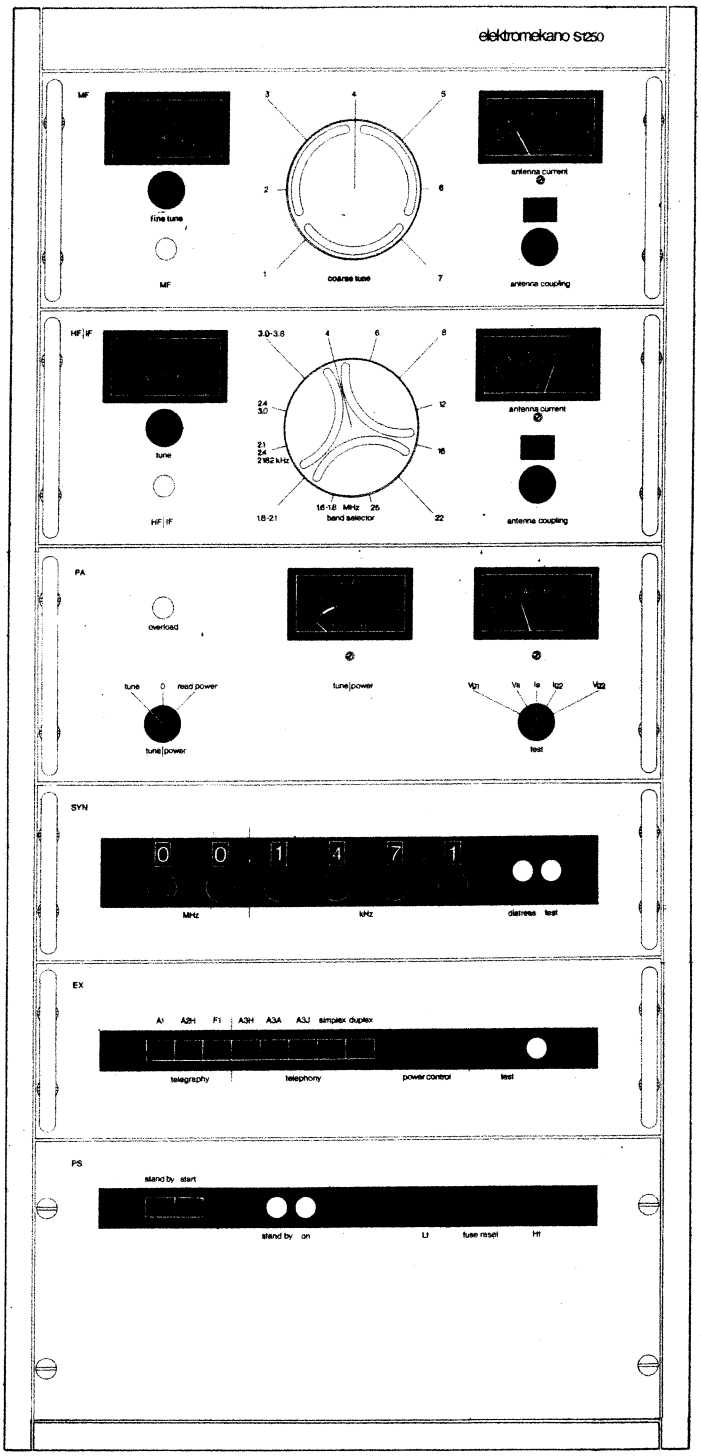


instruction manual

MAIN RADIO TELEGRAPH AND TELEPHONE TRANSMITTER

elektromekano S1250

part 2. diagrams



1980-10

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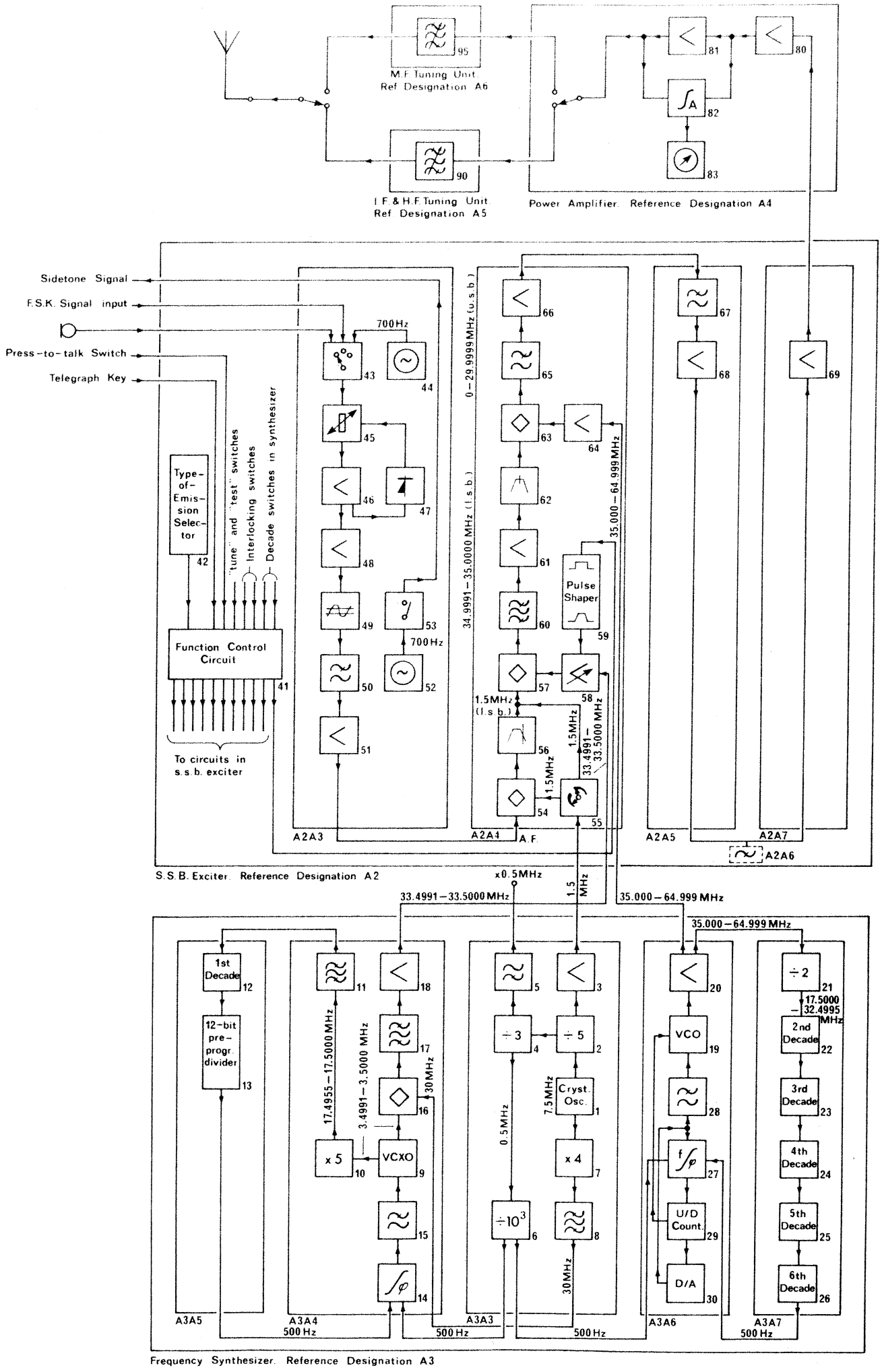
Part 2 of the Instruction Manual

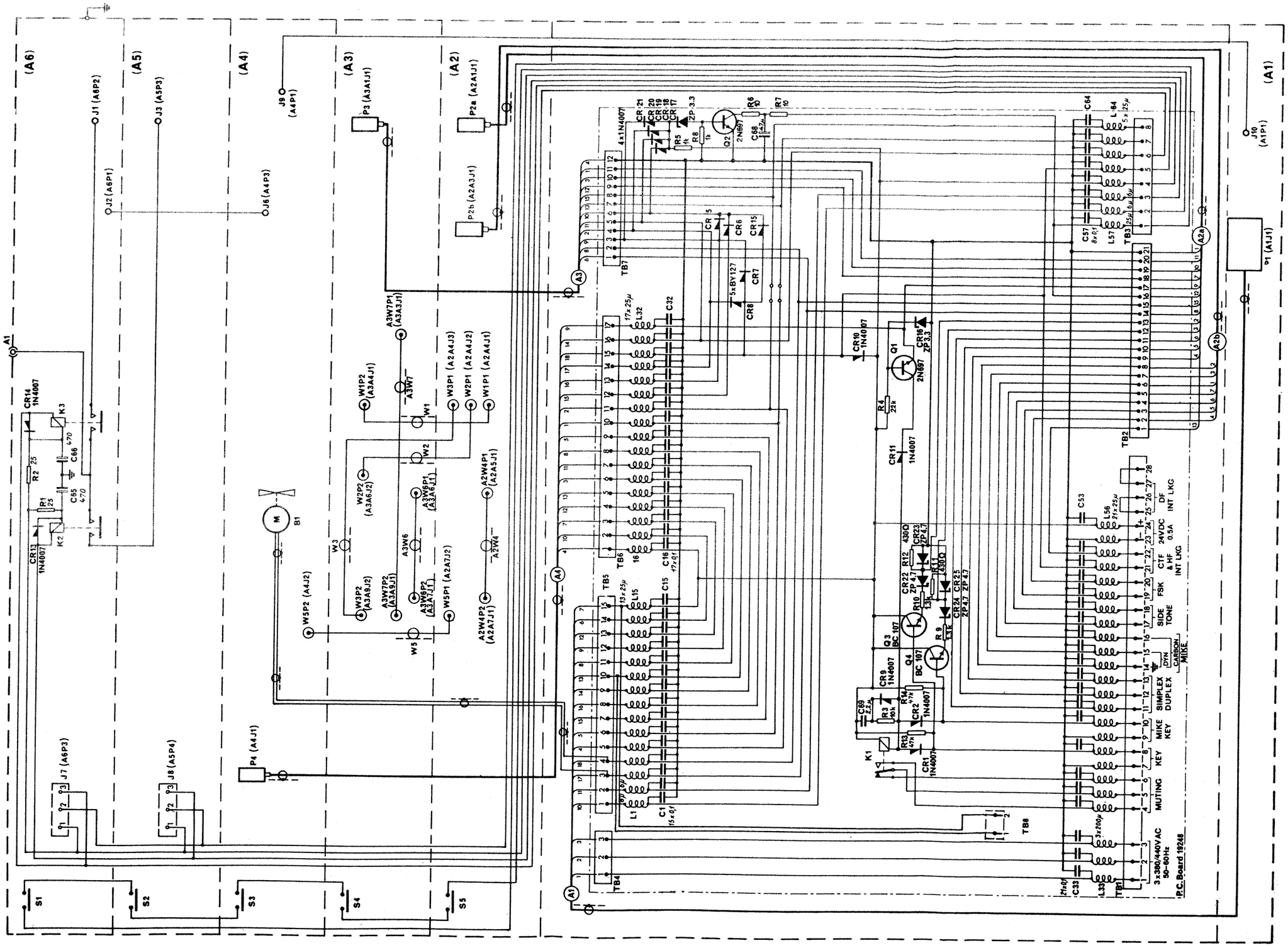
For the Sections 1 to 9, see Part 1 of the Instruction Manual

SECTION 10. - CIRCUIT DIAGRAMS, PHOTOS AND DRAWINGS



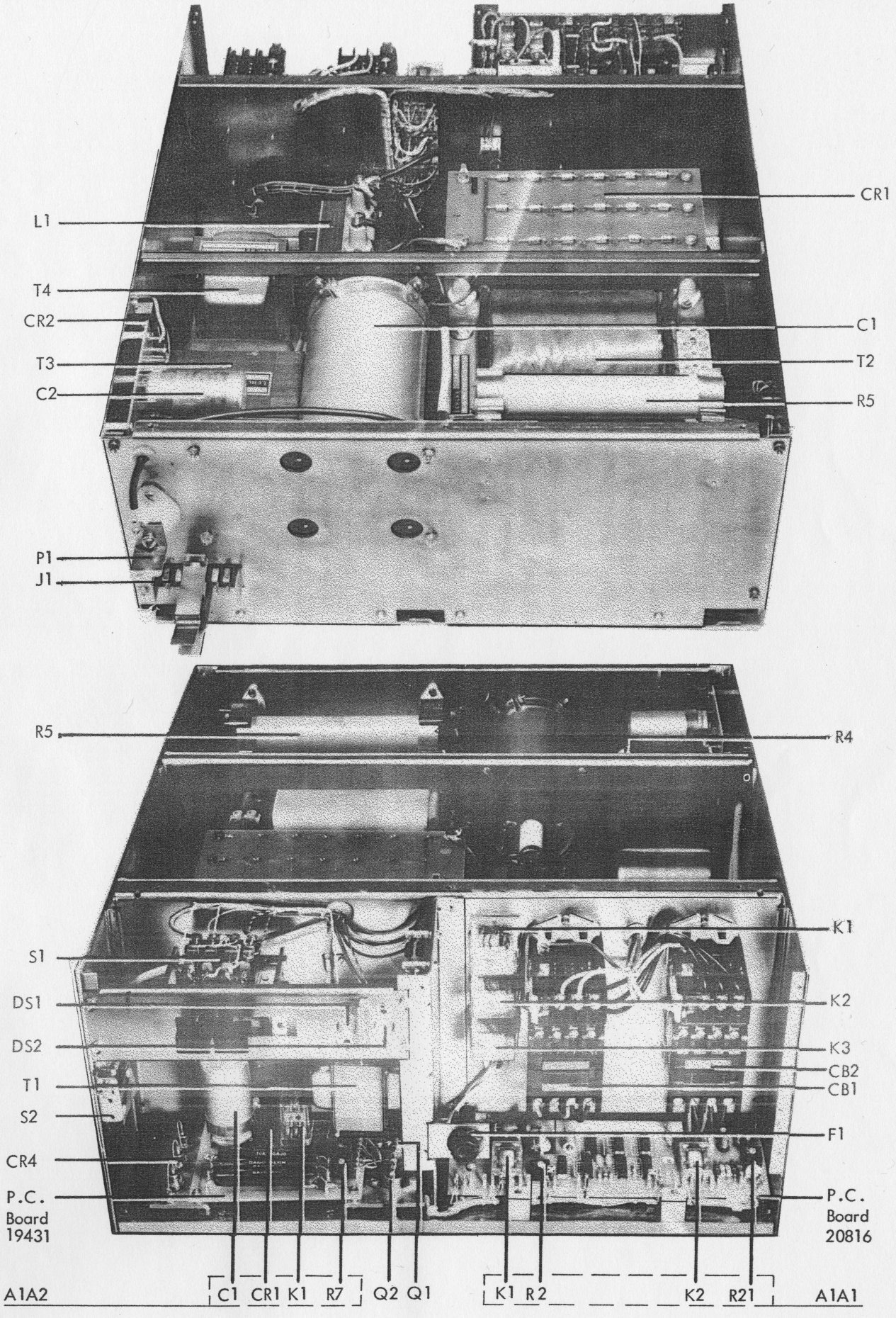
S 1250 Diagr. No. 4050/6-70

Block Diagram of Radio Telegraph and Telephone Transmitter



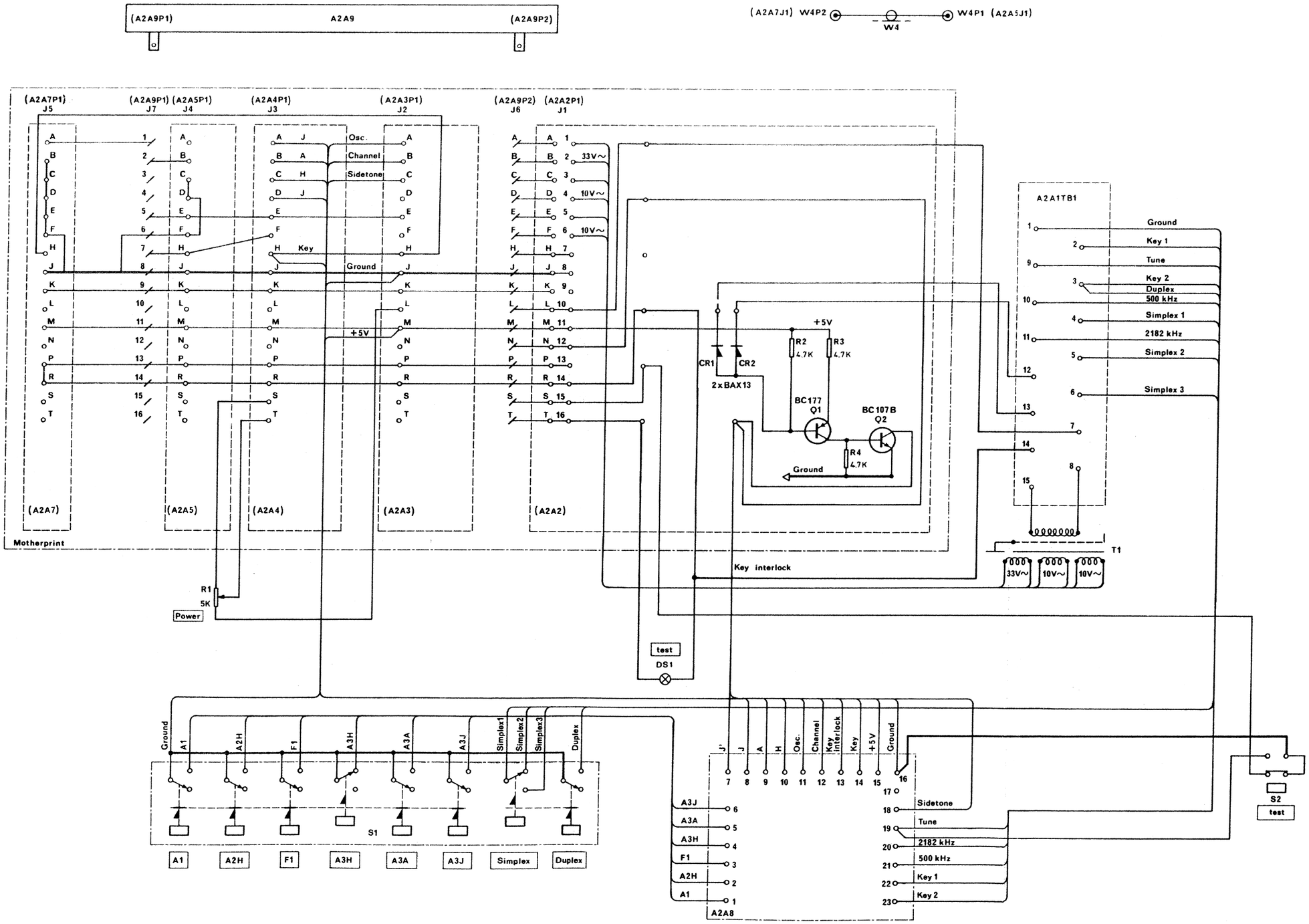
Unless otherwise specified: –
All resistance values are in ohms.
All capacitance values are in microfarads.
All inductance values are in henries.

Cabinet Rack Wiring



Main Power Supply Assembly

Ref. Designations A1, A1A1 and A1A2



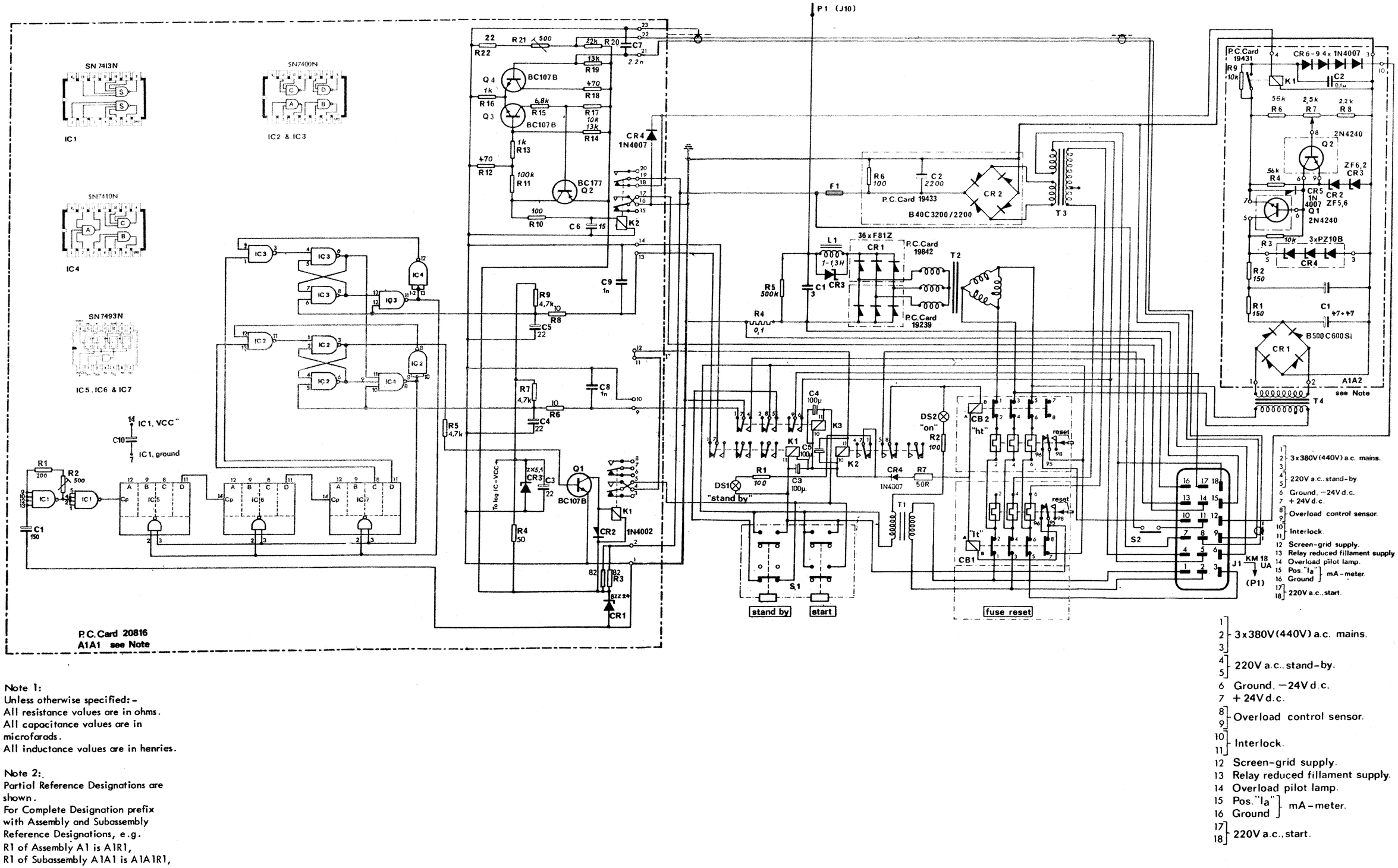
Note 1:
Unless otherwise specified:-
All resistance values are in ohms.
All capacitance values are in microfarads.
All inductance values are in henries.

Note 2:
Partial Reference Designations are shown.
For Complete Designation prefix with Assembly and Subassembly Reference Designations.

S 1250 Diagr.No. 4056/7.71

Single-Sideband Exciter Panel-and-Chassis Assembly

Ref. Designation A2



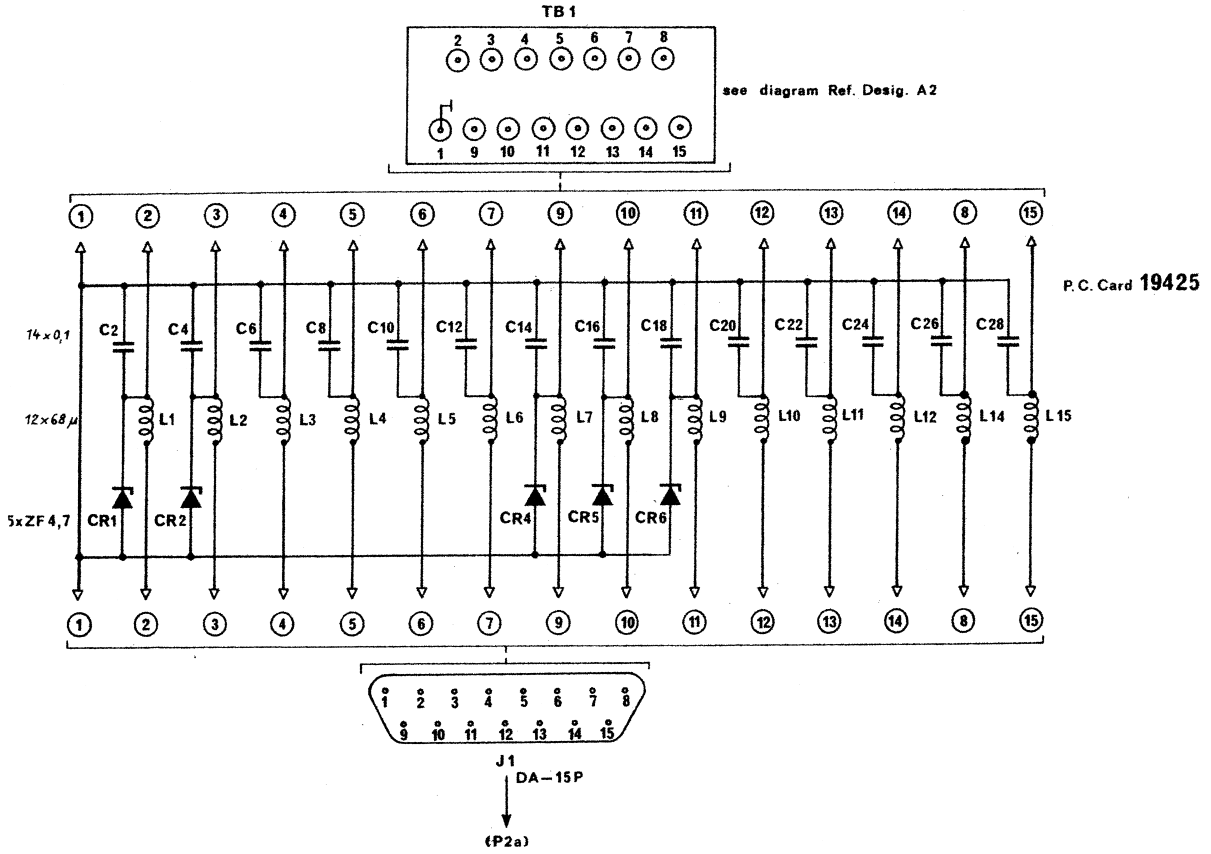
Note 1:
Unless otherwise specified:-
All resistance values are in ohms.
All capacitance values are in microfarads.
All inductance values are in henries.

Note 2:
Partial Reference Designations are shown.
For Complete Designation prefix with Assembly and Subassembly Reference Designations, e.g.
R1 of Assembly A1 is A1R1,
R1 of Subassembly A1A1 is A1A1R1,
etc.

1 } 3x380V(440V) a.c. mains.
2
3
4 } 220V a.c., stand-by.
5
6 Ground, −24V d.c.
7 +24V d.c.
8 } Overload control sensor.
9
10 } Interlock.
11
12 Screen-grid supply.
13 Relay reduced fillament supply.
14 Overload pilot lamp.
15 Pos. "Ia" } mA-meter.
16 Ground
17 } 220V a.c., start.
18

Main Power Supply Assembly

Ref. Designations A1, A1A1 and A1A2

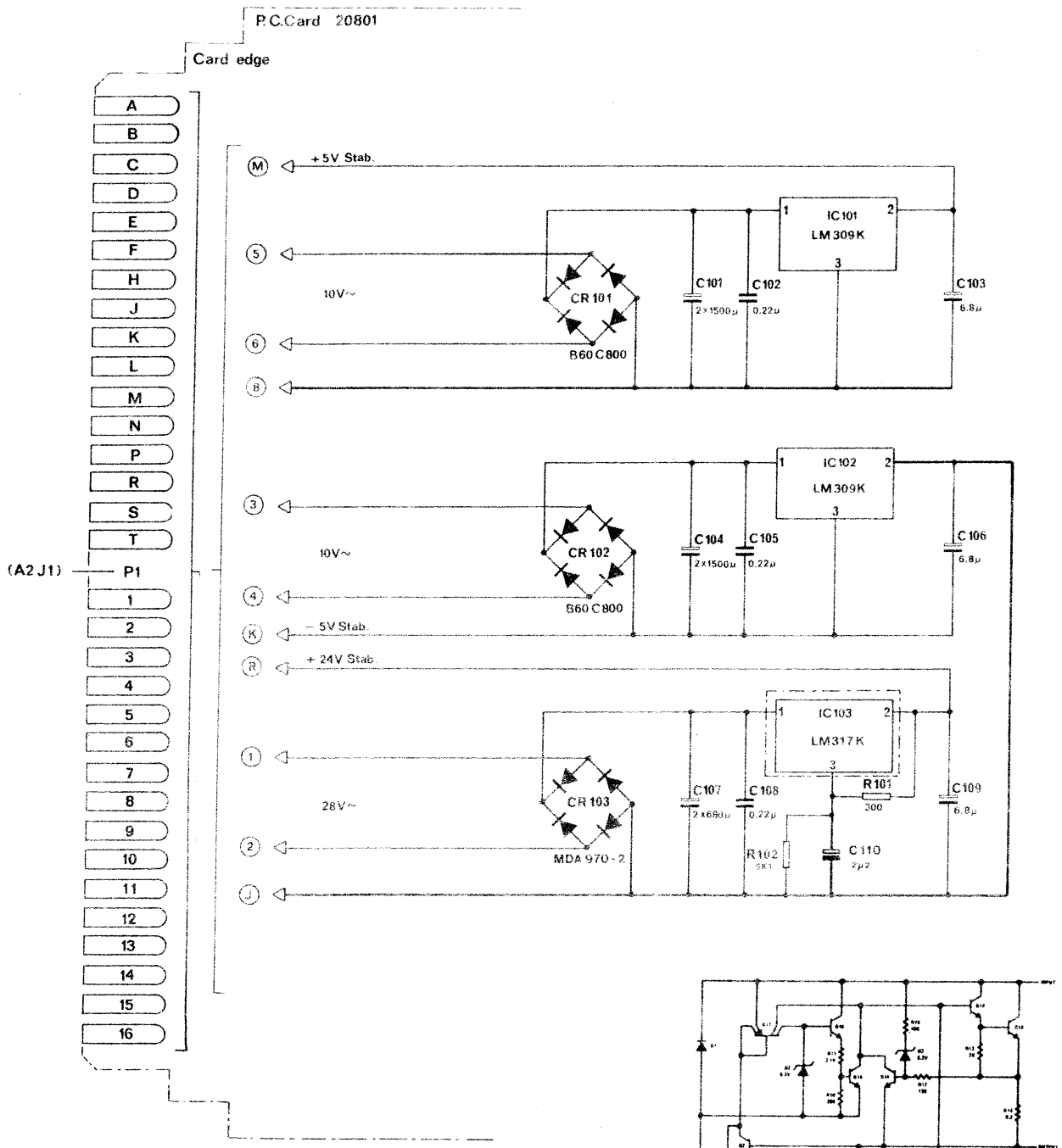


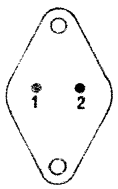
Note 1:
Unless otherwise specified:-
All resistance values are in ohms.
All capacitance values are in microfarads.
All inductance values are in henries.

Note 2:
Partial Reference Designations are shown.
For Complete Designation prefix with Assembly and Subassembly Reference Designations.

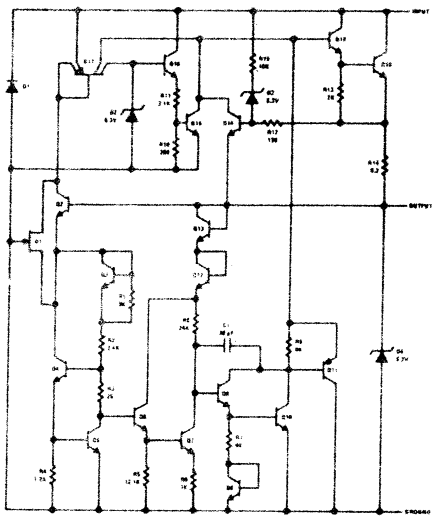
Radio-Frequency Filter Circuits for External Wiring

Ref. Designation A2A1





IC101, 102 & 103
(Bottom View)



IC 101, 102
LM 309K
Schematic Diagram

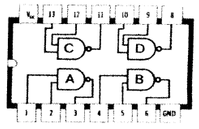
S.S.B. Exciter Power Supply

S 1250 DIAG No. 4213/1980-10

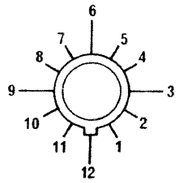
Ref. Designation A2A2

P.C. CARD 19428

SN7400N



IC1



IC2 & IC3

Tune/A2H osc. | Channel selector | Compression ampl. | AF Ampl. | Clipper | Filter

P1 (A2J2): A B C D E F H J K L M N P R S T

M +5 V
A Osc.
J Ground
B Channel
P
L
K −5 V
E AF out
C Sidetone act.
H Key out

R10 470 · R11 4,7k · R9 4,7k · R14 10k · R3 33k · R1 33k · R2 33k · R6 10k · R7 10k · R4 10k · R5 10k · R8 4,7k · C1 10n · C2 10n · C3 10n · C4 47 · C5 0,1 · Q1 BC107B · Q2 BC107B · Q3 BC107B · Q4 BC107B · IC1 (A B C D) · CR2 ZF4,7 · C6 47

R27 10k · Q7 2N5458 · R17 5,6k · R18 5,6k · R19 5,6k · R20 12k · Q6 2N5458 · R16 100k · Q5 2N5458 · R15 100k · C13 2,2 · C10 1n · R32 470 · R31 3,3k · C18 47 · R35 15k · R36 6,8k · C24 10 · R38 100 · R40 2,2k · R37 1,2k · Q15 BC177 · Q16 BC107B · R50 22k · C21 2,2 · C22 2,2 · C23 8,2n · CR1 BAX13 · IC2 · R26 22k · R29 180 · R34 56 · R33 1,2k · R25 10k · R28 1,2k · C8 2,2 · C7 2,2 · C9 2,2 · C11 2,2 · C12 22 · C17 47 · C19 47

R43 330 · R42 560 · Q8 BC107B · R41 56 · R44 1k · R39 1,2k · C25 47 · C26 47 · C27 10 · C28 47 · R51 1k · R49 1k · C29 47 · R48 1k · R47 470 · IC3 · L3 2,5m · Q9 BC107B · C31 47 · C32 1 · C33 1 · C34 47 · C3 47 · R56 1k · R55 1k

Set FSK tone level R12 5k · Set speech level R13 5k · R74 510 · R23 680 · R24 680 · R22 4,7k · C14 2,2 · C16 33n · C15 33n · C20 33n · L1 68µ · L2 68µ · R75 10k

J1−"1" MIC. CAR. · J1−"2" MIC. DYN. · J1−"3" · J1−"4" TONE SHIFT · J1−"5" · J1−"6" SIDE TONE · J1−"7"

J1(P2b) DA-15S · R46 4,7k · R45 5k Set clipping level · R70 10k · R52 9K9 · R79 NTC 15K · R53 7K5 · Set output level R54 500

R65 10k · R60 470 · C42 22 · R66 10k · R68 10k · R63 10k · Q13 BC107B · C41 2,2 · C44 2,2 · R58 56k · R64 10k · R72 5,6k · Q14 2N5458 · R69 330 · R57 56k · R59 56k · Q11 BC107B · Q12 BC107B · R67 10k · Q17 BC107B · L4 68µ · R73 56k · C43 0,1 · R71 1k · C45 0,1 · C36 10n · C37 10n · C38 10n · R61 10k · R62 10k · C39 47

Sidetone Osc. · Sidetone Key

Note 1:
Unless otherwise specified:-
All resistance values are in ohms.
All capacitance values are in microfarads.
All inductance values are in henries

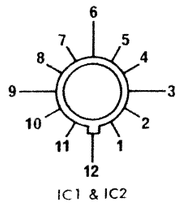
Note 2:
Partial Reference Designations are shown.
For Complete Designation prefix with Assembly and Subassembly Reference Designations.

Note 3:
Gates, flip-flops, etc. contained in an integrated-circuit package (IC) are identified by ref. designations shown on the individual logic-circuit symbols.

S 1250 DIAG No. 4052/1980-10

Audio-Frequency Signal Processing Circuits

Ref. Designation A2A3



IC1 & IC2

P.C. CARD
18816

P1
A
B
C
D
E
F
H
J
K
L
M
N
P
R
S
T

A2J3

Balanced Mod. | X-filter | Balanced Mix | Ampl. | X-filter | Balanced Mix. | Filter | Ampl.

F 0-30 MHz
M +5V
E AF
J Ground
K -5V
A J
B A
C H
D J'
T
H Key
S

L1 6,8µ
L2 6,8µ
L3 68µ
L4 68µ
L5 68µ
L6 68µ
L7 68µ
L8 68µ
L9 6,8µ
L10 6,8µ
L11 6,8µ
L12 470µH
FL1
T1
T2
T3
T4
T5
T6
T7
T8
IC1
IC2
Y1
Y2
Q1 BFY78
Q2 BFY78
Q3 BFY78
Q4 BC177
Q5 BC107B
Q6 BC177
CR1
CR2
CR3
CR4
CR5 5082-2815
CR6 4 x BAX13
CR7
CR8
CR9
CR10 BAX13
4xBA244
RT1 330
R1 220
R2 100
R3 100
R4 11K
R5 470
R6 47
R7 2,5k
R8 620
R9 3,9k
R10 22
R11 1k
R12 220
R13 180
R14 12k
R15 100
R16 47
R17 470
R18 100
R19 47
R20 620
R21 10
R22 270
R24 1k
R25 100
R26 47
R27 180
R28 120
R29 4,7k
R30 22
R31 1k
R32 39k
R33 10
R34 12k
R35 18k
R36 4,7k
R37 1k
R38 2,2k
R39 1k
R40 100k
R41 50k
R42 270
R43 200
R44 11K
C2 8,2n
C3 82n
C4 8,2n
C5 39n
C6 39n
C7 82n
C8 8 x 0,47
C9
C10
C11
C12
C13
C14
C15
C16 8,2n
C17 39n
C18 39n
C19 18p
C20 18p
C21 8,2n
C22 82p
C23 8,2n
C24 8,2n
C25 8,2n
C26 8,2n
C27 2-10p
C28
C29
C30 5p
C31 8,2n
C32 1n
C33 8,2n
C34 8,2n
C35 8,2n
C36 4,7p
C37 10p
C38 4,7p
C39 82n
C40 1n
C41 39n
C42 82n
C43 0,47
C45 8,2n
C47 33p
C48 82n

UG-290A/U (W3P1)J3 1,5MHz
UG-290A/U J1(W1P1) 33,5MHz
UG-290A/U J2(W2P1) 35-65 MHz
5V
-5V
Ground

Note 1:
Unless otherwise specified:-
All resistance values are in ohms.
All capacitance values are in microfarads.
All inductance values are in henries.

Note 2:
Partial Reference Designations are shown.
For Complete Designation prefix with Assembly and Subassembly Reference Designations.

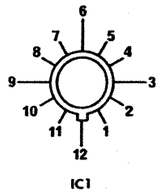
Note 3:
Gates, flip-flops, etc. contained in an integrated-circuit package (IC) are identified by ref. designations shown on the individual logic-circuit symbols.

Carrier reinsertion circuit

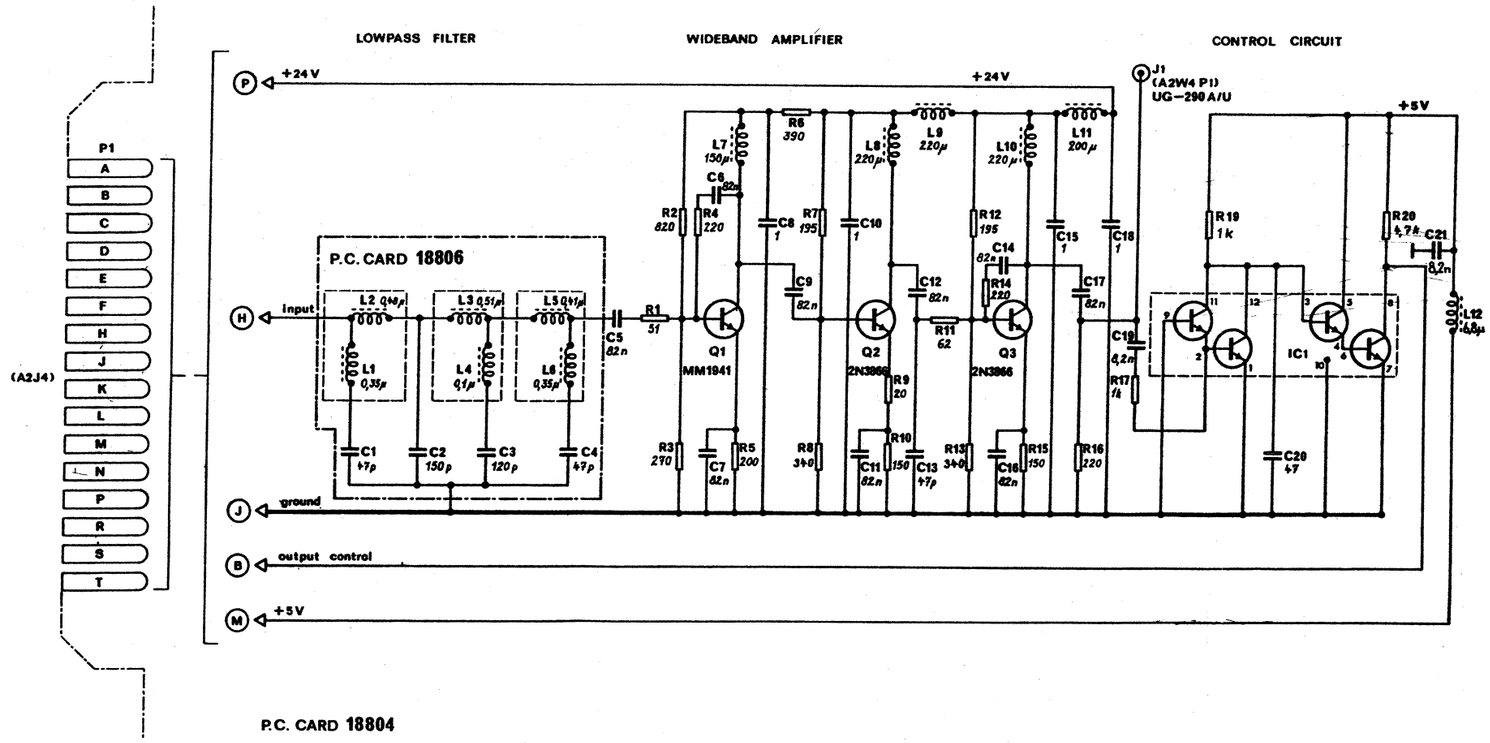
Pulseshaping circuit

Modulator, Filter and Mixer Circuits

Ref. Designation A2A4



IC1

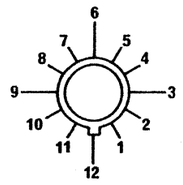


Note 1:
Unless otherwise specified:-
All resistance values are in ohms.
All capacitance values are in microfarads.
All inductance values are in henries.

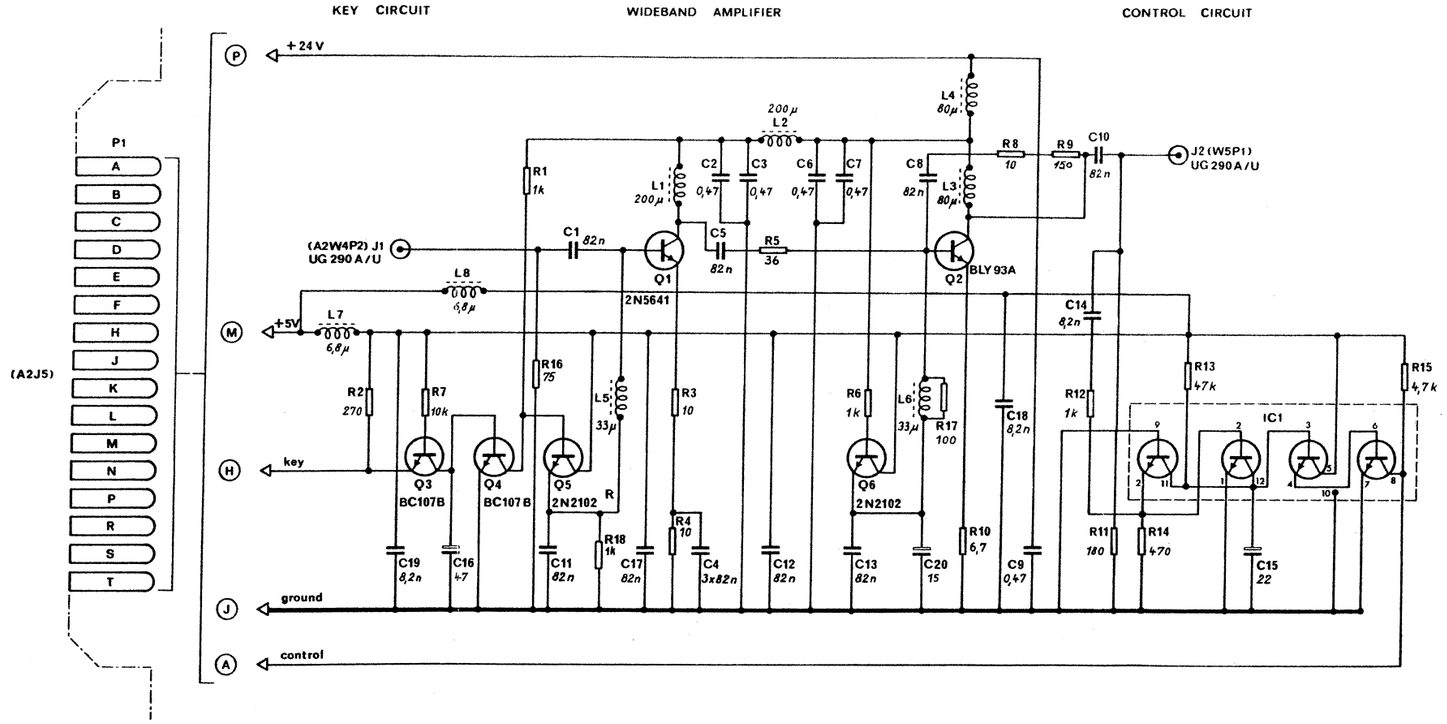
Note 2:
Partial Reference Designations are shown.
For Complete Designation prefix with Assembly and Subassembly Reference Designations.

Three-Stage Wide-Band Amplifier

Ref. Designation A2A5



IC1



P.C.CARD **18803**

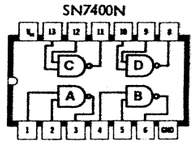
Note 1:
Unless otherwise specified:-
All resistance values are in ohms.
All capacitance values are in microfarads.
All inductance values are in henries.

Note 2:
Partial Reference Designations are shown.
For Complete Designation prefix with Assembly and Subassembly Reference Designations.

Two-Stage Wide-Band Amplifier

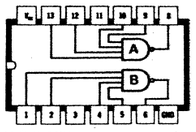
Ref. Designation A2A7

SN7400N

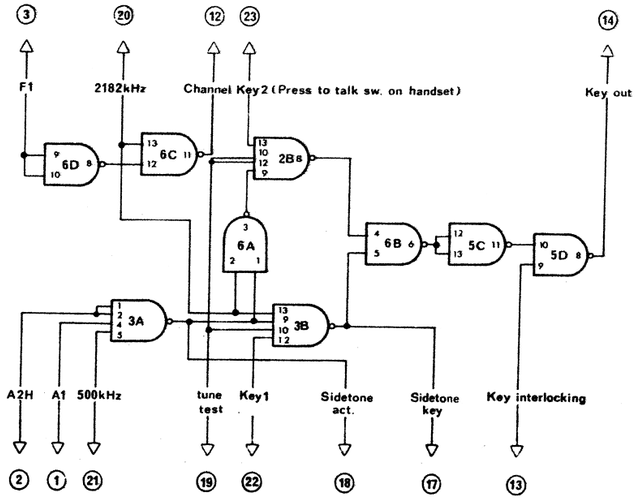


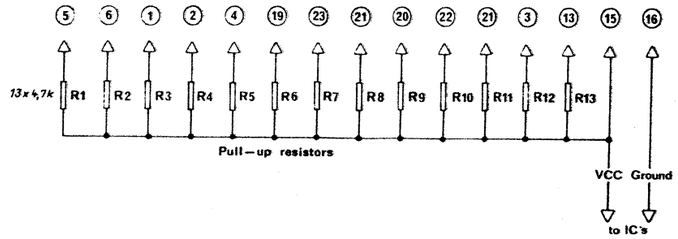
IC1, IC4, IC5 & IC6

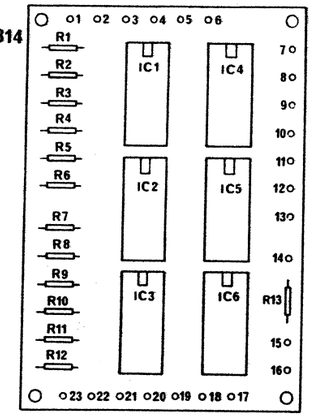
SN7420N

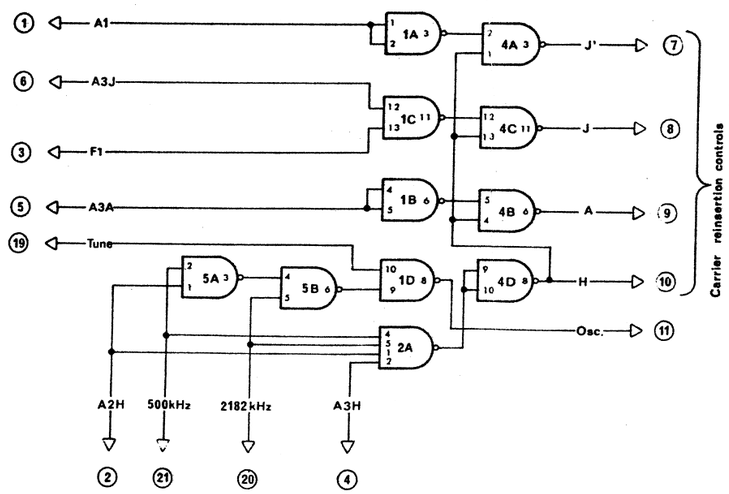


IC2 & IC3









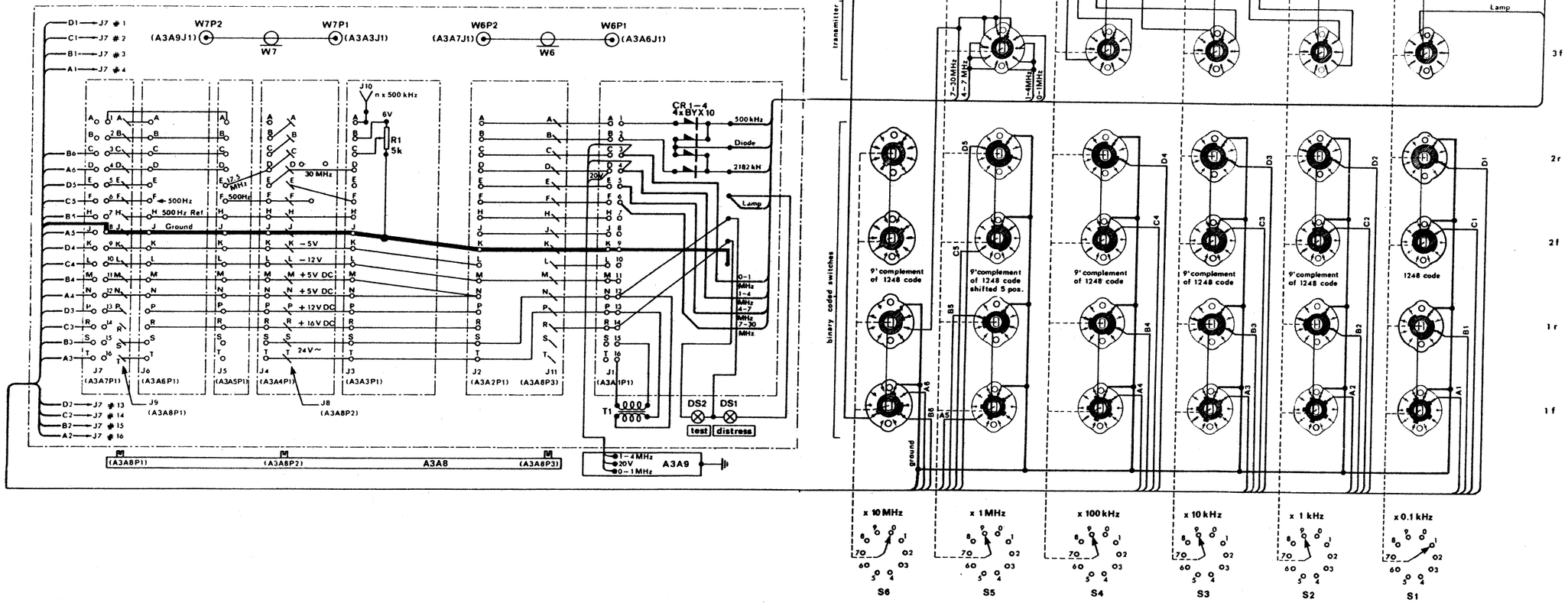
Note 1:
Unless otherwise specified:-
All resistance values are in ohms.
All capacitance values are in microfarads.
All inductance values are in henries.

Note 2:
Partial Reference Designations are shown.
For Complete Designation prefix with Assembly and Subassembly Reference Designations.

Note 3:
Gates, flip-flops, etc. contained in an integrated-circuit package (IC) are identified by ref. designations shown on the individual logic-circuit symbols.

Function Control Circuit

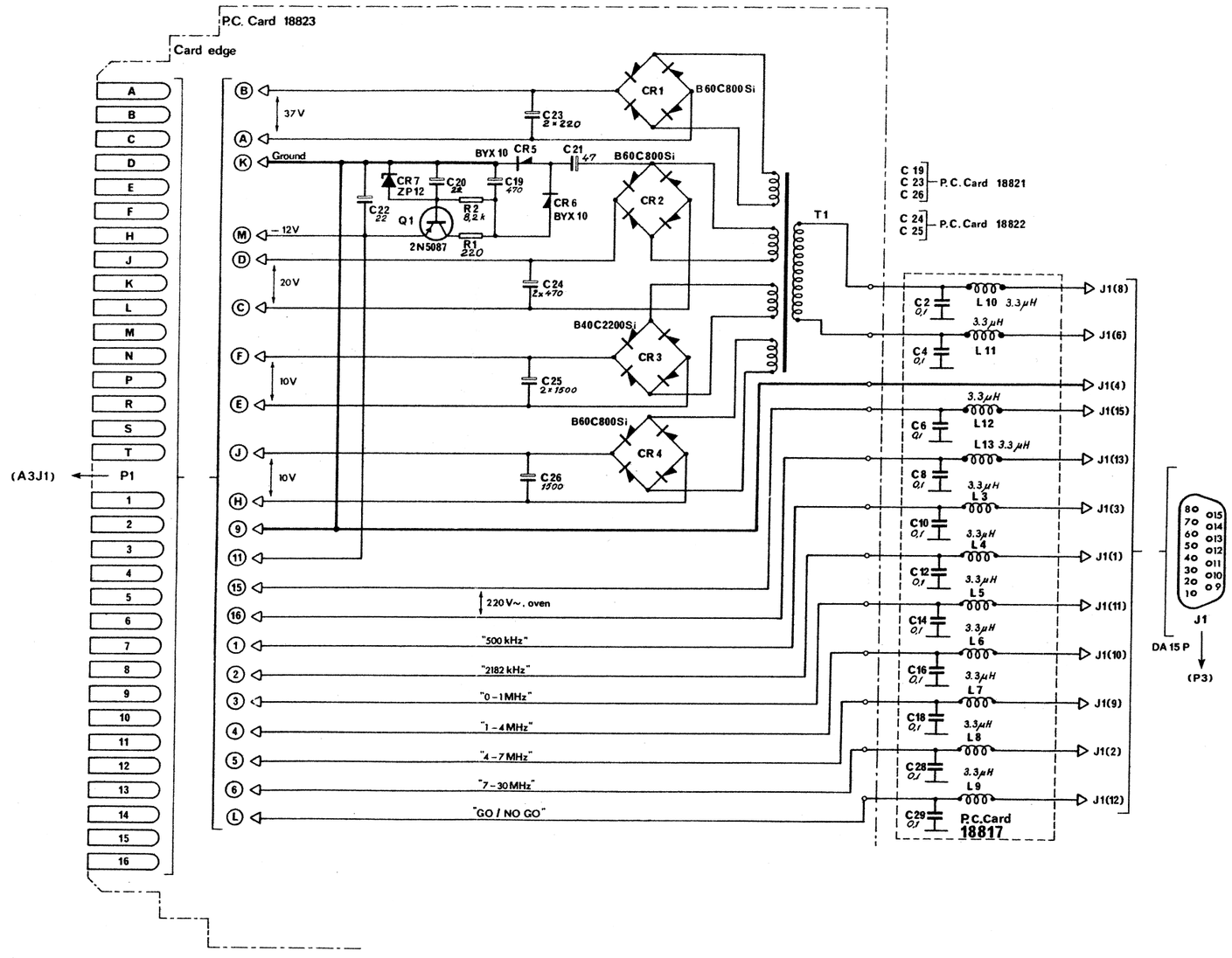
Ref. Designation A2A8



S 1250 Diagr.No.4053/1974-02

Frequency Synthesizer Panel-and-Chassis Assembly

Ref. Designation A3



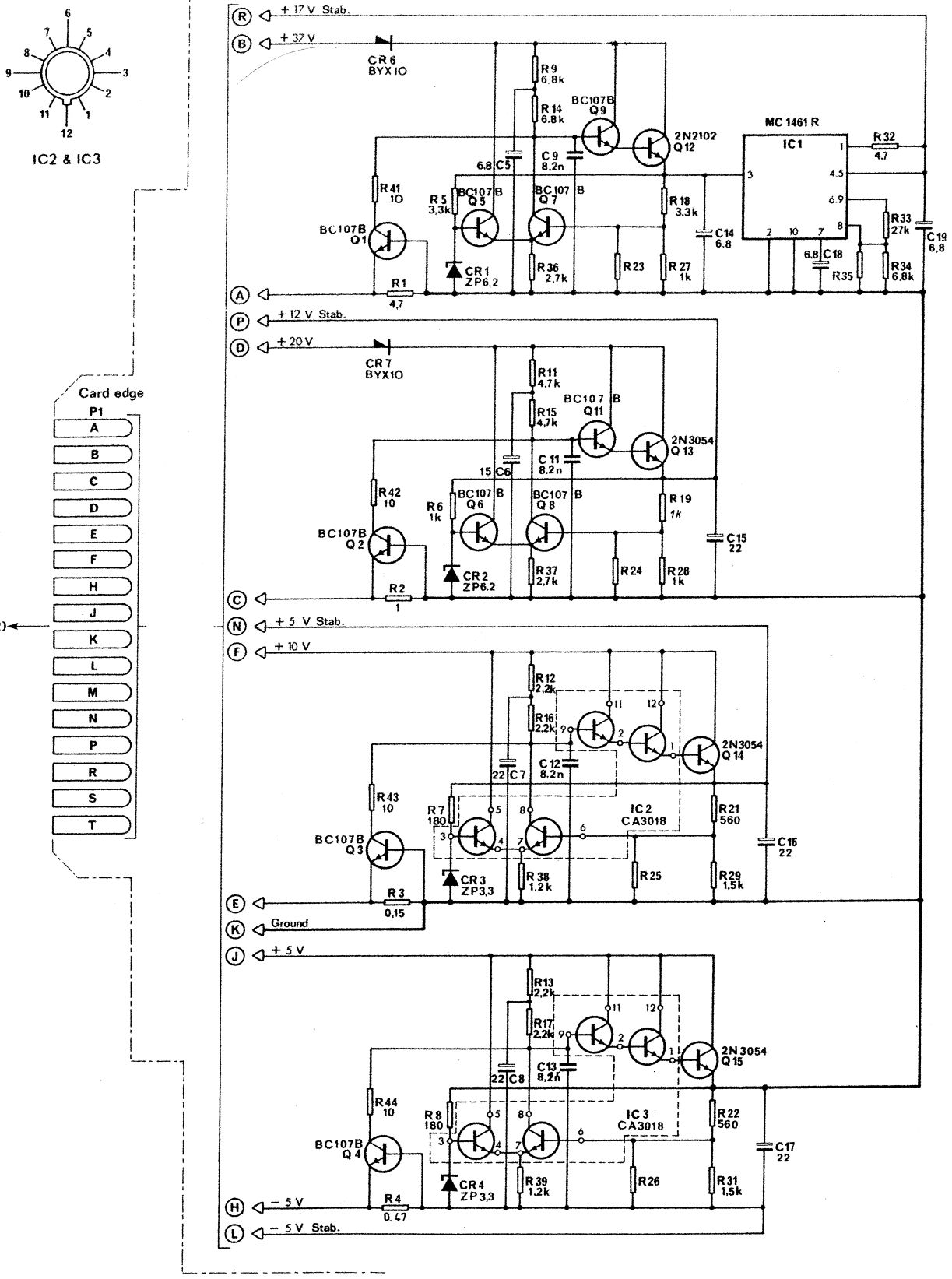
Note 1:
Unless otherwise specified:-
All resistance values are in ohms.
All capacitance values are in microfarads.
All inductance values are in henries.

Note 2:
Partial Reference Designations are shown.
For Complete Designation prefix with Assembly and Subassembly Reference Designations.

S 1250 DIAG No.4042/1973-02

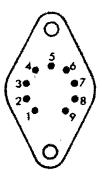
Rectifier Circuits

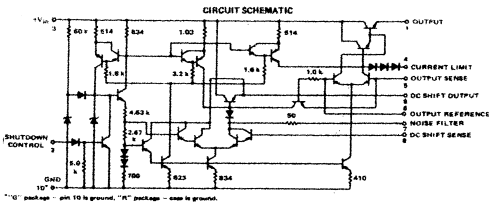
Ref. Designation A3A1



Note 1:
Unless otherwise specified:-
All resistance values are in ohms.
All capacitance values are in microfarads.
All inductance values are in henries.

Note 2:
Partial Reference Designations are shown.
For Complete Designation prefix with Assembly and Subassembly Reference Designations.



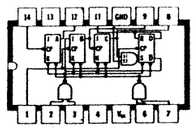


MC1461R

Voltage-Regulator Circuits

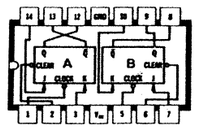
Ref. Designation A3A2

SN7490N



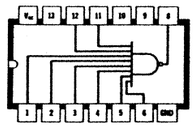
IC2, IC4, IC5 & IC6

SN7473N

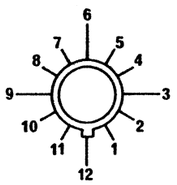


IC3

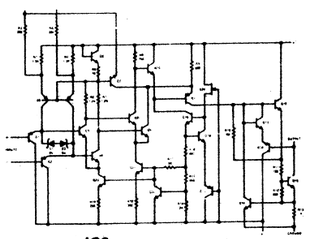
SN7430N



IC7



IC1, IC9 & IC10

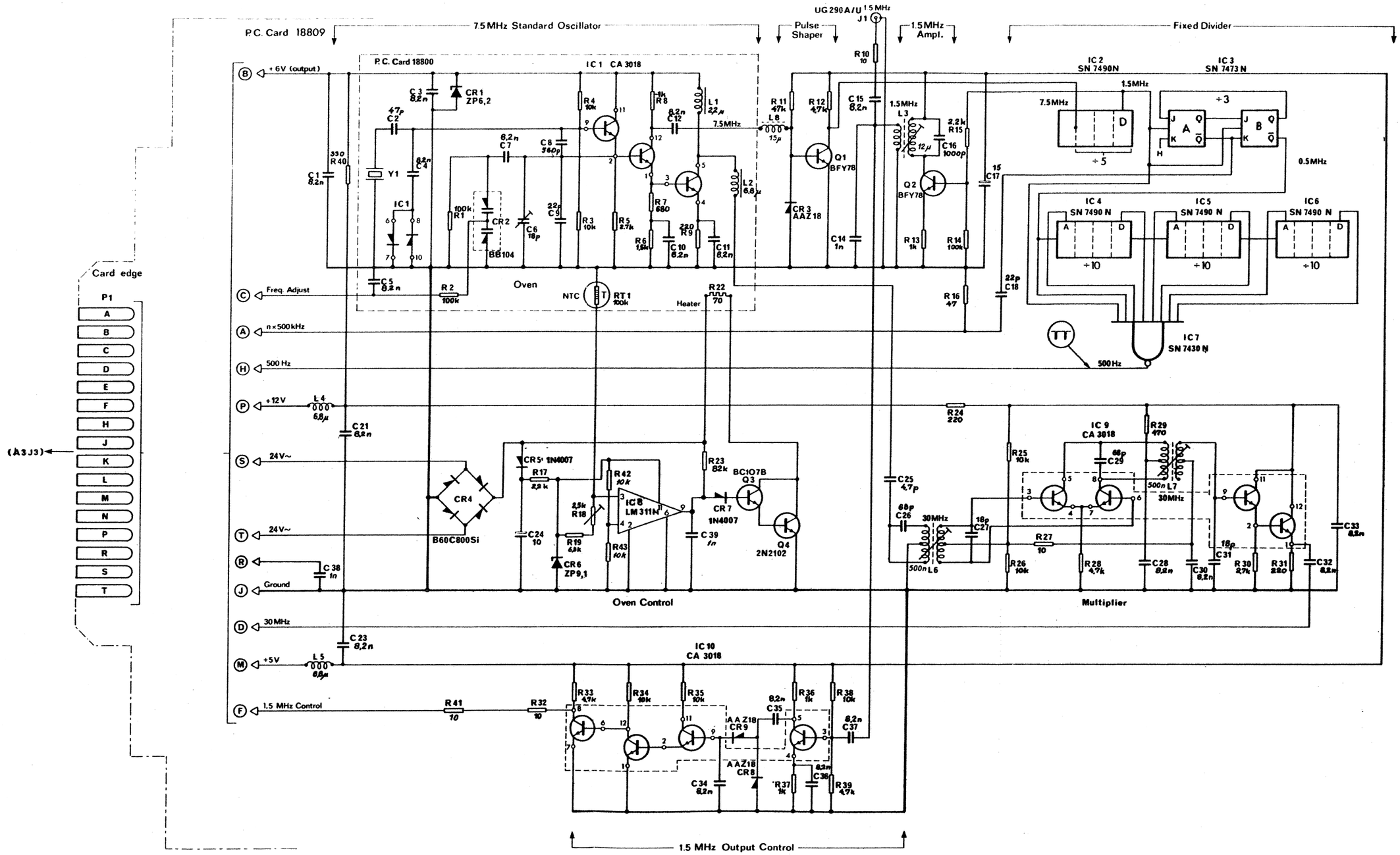


IC8

Note 1:
Unless otherwise specified:-
All resistance values are in ohms.
All capacitance values are in microfarads.
All inductance values are in henries.

Note 2:
Partial Reference Designations are shown.
For Complete Designation prefix with Assembly and Subassembly Reference Designations.

Note 3:
Gates, flip-flops, etc. contained in an integrated-circuit package (IC) are identified by ref. designations shown on the individual logic-circuit symbols.

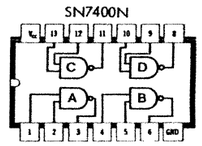


H = +5V
L = 0V

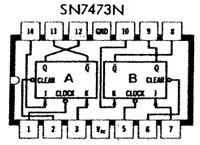
S 1250 DIAG No.4247/1973-02

Frequency Standard

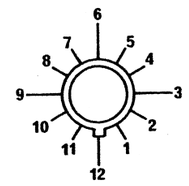
Ref. Designation A3A3



IC3



IC4



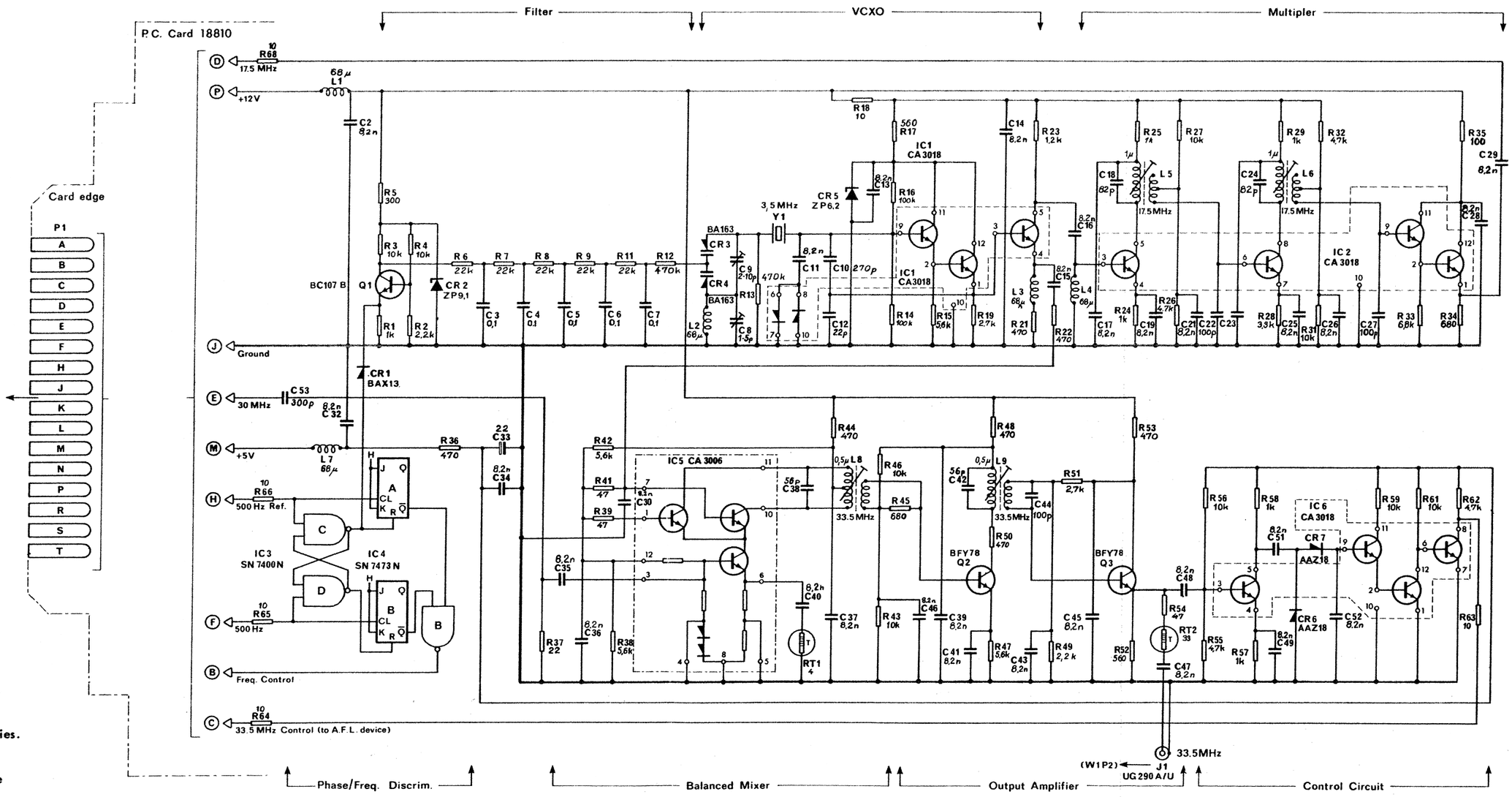
IC1, IC2, IC5 & IC6

H = +5V
L = 0V

Note 1:
Unless otherwise specified:-
All resistance values are in ohms.
All capacitance values are in microfarads.
All inductance values are in henries.

Note 2:
Partial Reference Designations are shown.
For Complete Designation prefix with Assembly and Subassembly Reference Designations.

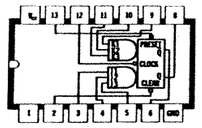
Note 3:
Gates, flip-flops, etc. contained in an integrated-circuit package (IC) are identified by ref. designations shown on the individual logic-circuit symbols.



33.4991-33.5000 MHz Phase-Locked Loop

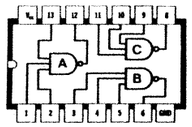
Ref. Designation A3A4

SN74H72N



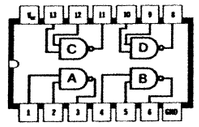
IC D2, D3, D4, D5 & D6

SN74H11N



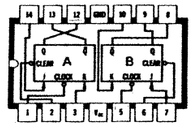
IC E3

SN74H00N



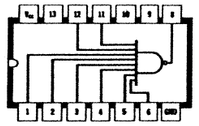
IC E2 & E4

SN7473N



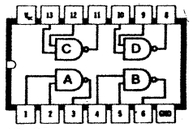
IC B2, B3, B4, B5, B6 & C4

SN7430N



IC C2

SN7400N



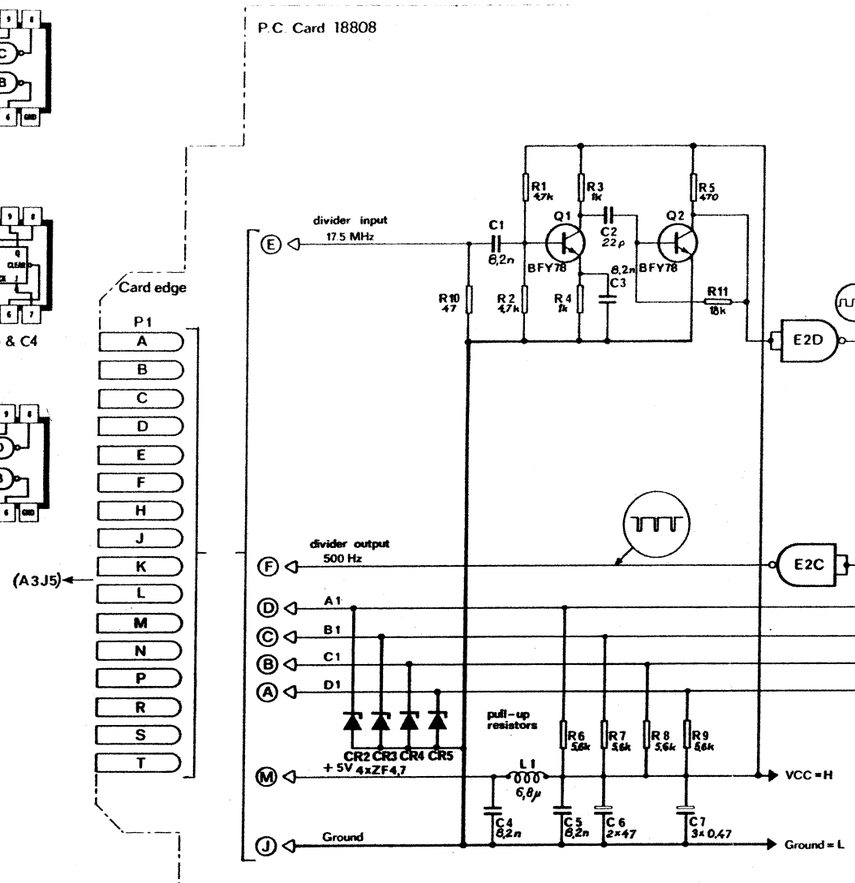
IC C3

H = +5V
L = 0V

Note 1:
Unless otherwise specified:-
All resistance values are in ohms.
All capacitance values are in microfarads.
All inductance values are in henries.

Note 2:
Partial Reference Designations are shown.
For Complete Designation prefix with Assembly and Subassembly Reference Designations.

Note 3:
Gates, flip-flops, etc. contained in an integrated-circuit package (IC) are identified by ref. designations shown on the individual logic-circuit symbols, e.g.
E3C is gate C contained in ICE3.
The first letter and the following number are also used as coordinates to specify the physical location of the IC on the p.c. card.



ripple-through divider

0.1 kHz dec. Sw. S1				
Dial	A1	B1	C1	D1
0	1	0	0	1
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	1	1	0
8	1	1	1	0
9	0	0	0	1

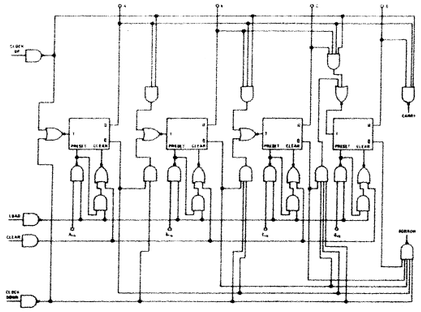
Truth Table for the preset lines.

S1 Dial	x	y	z
0	0	0	0
0	1	0	0
0	0	1	0
0	1	1	1
≠ 0	0	0	0
≠ 0	1	0	0
≠ 0	0	1	1
≠ 0	1	1	1

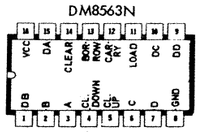
33.4991-33.5000 MHz Variable-Ratio Frequency Divider

Ref. Designation A3A5

P.C. Card 18812

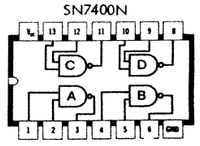


DM8563N



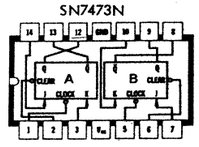
IC4 & IC5

SN7400N

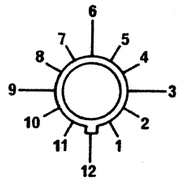


IC1, IC3 & IC6

SN7473N



IC2



IC8

Card edge

P1

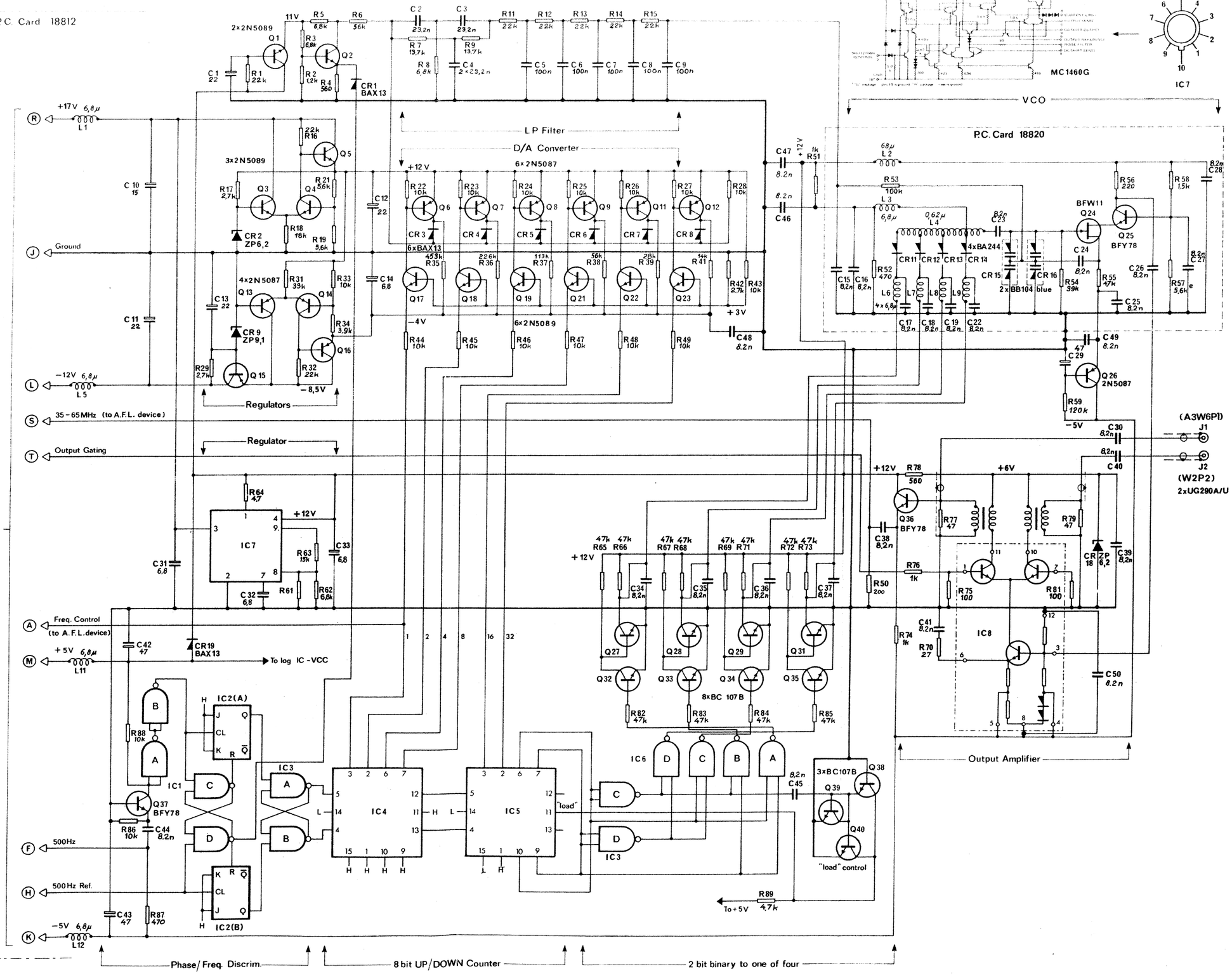
A B C D E F H J K L M N P R S T

(A3J6

Note 1:
Unless otherwise specified:-
All resistance values are in ohms.
All capacitance values are in microfarads.
All inductance values are in henries

Note 2:
Partial Reference Designations are shown.
For Complete Designation prefix with Assembly and Subassembly Reference Designations.

Note 3:
Gates, flip-flops, etc. contained in an integrated-circuit package (IC) are identified by ref. designations shown on the individual logic-circuit symbols.

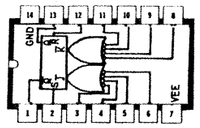


35.000-64.999 MHz Phase-Locked Loop

Ref. Designation A3A6

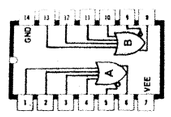
P.C. Card 18813

MC1013P



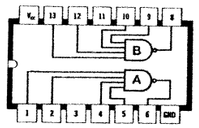
IC A1, A2, A3, A4, A5 & A6

MC1004P



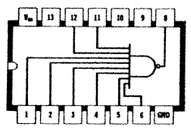
IC B1, B2, B3, B4, B5 & B6

SN74H20N



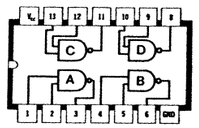
IC D1

SN74H30N



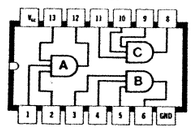
IC E1

SN7400N



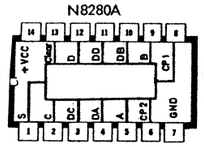
IC F3, H2 & H3

SN7410N



IC F2

N8280A



IC D2, E2, F1 & H1

Card edge

A B C D E F H J K L M N P R S T

P1

(A3J7) ← 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

Divider input 35 – 65 MHz

(A3W3P2) UG290A/U ← J1 — C1 8,2n — R1 7,5k

B6B B6A A6 A5 A4 A3 A2 A1 D' B4B B3B B2B B1B B1A

500 Hz — Divider output 500 Hz

A2 B2 C2 D2 — 18 x 4,7k R8 R9 R10 R11 — Pull-down resistors

B5B B5A B4A 2nd decade B3A B2A strobe line

−5V — 6,8µ L2 — C4 8,2n C6 22

H = 0V L = −5V

H = +5V L = 0V

Ground — C3 8,2n C5 22 — +5V — 6,8µ L1

VEE — R5 470 CR1 BAX13 — R7 470 CR7 BAX13 — R6 1k CR5 BAX13 CR6 BAX13

Ground — BA 244 CR22 — BFY78 Q1 — R2 1,8k — R26 470 — ECL–TTL interface

BFY78 Q2 — R4 1,8k — R27 470 — ECL–TTL interface — BAX 13 CR3 BAX 13 CR4 — R3 470 — TTL–ECL interface

VCC

14 x ZF4,7 CR8 CR9 CR10 CR11 — R12 R13 R14 R15 — 3 rd decade

A3 B3 C3 D3 — CR12 CR13 CR14 CR15 — R16 R17 R18 R19 — 4 th decade

A4 B4 C4 D4 — CR16 CR17 CR18 CR19 — R20 R21 R22 R23 — 5 th decade

A5 B5 C5 D5 — CR20 CR21 — R24 R25 — 6 th decade — Pull-up resistors

D1A D1B — strobe line — H

E1

D5 B5 C5 A5 A6' B6' C6' — F3C F3B F3D H2D H2B H2C H3C H3B H3D F2A H2D F2B F2C H3A F3A — carry carry — B6 A6 — Adder circuit

Truth Table for Adder Circuit

Switch pos.	Input					Output			Output frequency
S6 S5	A6 B6	A5 B5	C5 D5			A6 B6	C6		MHz
0 0	1 0	0 0	1 0			0 1	1		35
0 1	1 0	1 0	0 0			0 1	1		36
0 2	1 0	0 1	0 0			0 1	1		37
0 3	1 0	1 0	0 0			0 1	1		38
0 4	1 0	0 0	0 0			0 1	1		39
0 5	1 0	1 0	0 1			1 0	1		40
0 6	1 0	0 0	0 1			1 0	1		41
0 7	1 0	1 1	1 0			1 0	1		42
0 8	1 0	0 1	1 0			1 0	1		43
0 9	1 0	1 0	1 0			1 0	1		44
1 0	0 0	0 0	1 0			1 0	1		45
1 1	0 0	1 1	1 0			1 0	1		46
1 2	0 0	0 1	1 0			1 0	1		47
1 3	0 0	1 0	0 0			1 0	1		48
1 4	0 0	0 0	0 0			1 0	1		49
1 5	0 0	1 0	0 1			0 0	1		50
1 6	0 0	0 0	0 1			0 0	1		51
1 7	0 0	1 1	1 0			0 0	1		52
1 8	0 0	0 1	1 0			0 0	1		53
1 9	0 0	1 0	1 0			0 0	1		54
2 0	0 1	0 0	1 0			0 0	1		55
2 1	1 1	1 1	0 0			0 0	1		56
2 2	1 1	0 1	0 0			0 0	1		57
2 3	1 1	1 0	0 0			0 0	1		58
2 4	1 1	0 0	0 0			0 0	1		59
2 5	1 1	1 0	0 1			1 1	0		60
2 6	1 1	0 0	0 1			1 1	0		61
2 7	1 1	1 1	1 0			1 1	0		62
2 8	1 1	0 1	1 0			1 1	0		63
2 9	1 1	1 0	1 0			1 1	0		64
	0 = 0V		1 = +5V						

Truth Table for the preset lines.

	1 kHz dec. Sw. S2			10 kHz dec. Sw. S3			100 kHz dec. Sw. S4			1 MHz dec. Sw. S5			10 MHz dec. Sw. S6
Dial	A2	B2	C2	A3	B3	C3	A4	B4	C4	A5	B5	C5	A6	B6	
0	1	0	0	1	1	0	0	1	1	0	1	0	0	1	0
1	0	0	0	1	0	0	0	1	1	0	0	1	1	0	0
2	1	1	1	0	1	1	1	0	1	1	1	0	0	1	1
3	0	1	1	0	0	1	1	0	0	1	1	0	1	0	0
4	1	0	1	0	1	0	1	0	1	0	1	0	0	0	0
5	0	0	1	0	0	0	1	0	0	0	1	0	1	0	0
6	1	1	0	0	1	1	0	0	1	1	0	0	0	0	1
7	0	1	0	0	0	1	0	0	0	1	0	0	1	1	0
8	1	0	0	0	1	0	0	0	1	0	0	0	1	1	0
9	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	0 = 0V 1 = −5V			0 = 0V 1 = 5V											

Note 1:
Unless otherwise specified:–
All resistance values are in ohms.
All capacitance values are in microfarads.
All inductance values are in henries.

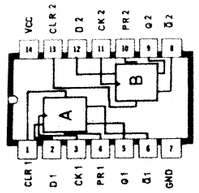
Note 2:
Partial Reference Designations are shown.
For Complete Designation prefix with Assembly and Subassembly Reference Designations.

Note 3:
Gates, flip-flops, etc. contained in an integrated-circuit package (IC) are identified by ref. designations shown on the individual logic-circuit symbols, e.g.
B3A is gate A contained in ICB3.
The first letter and the following number are also used as coordinates to specify the physical location of the IC on the p.c. card.

35.000–64.999 MHz Variable-Ratio Frequency Divider

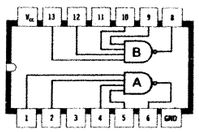
Ref. Designation A3A7

SN74S74



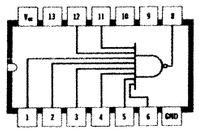
IC C2

SN74H20N



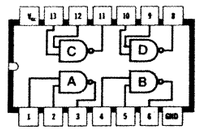
IC D1

SN74H30N



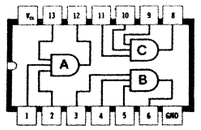
IC E1

SN7400N



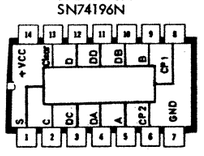
IC F3, H2 & H3

SN74S10N
SN7410N

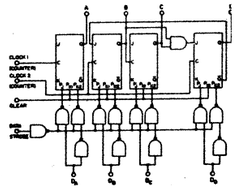


IC C1, F2

SN74S196N
SN74196N



IC B2, D2, E2, F1 & H1



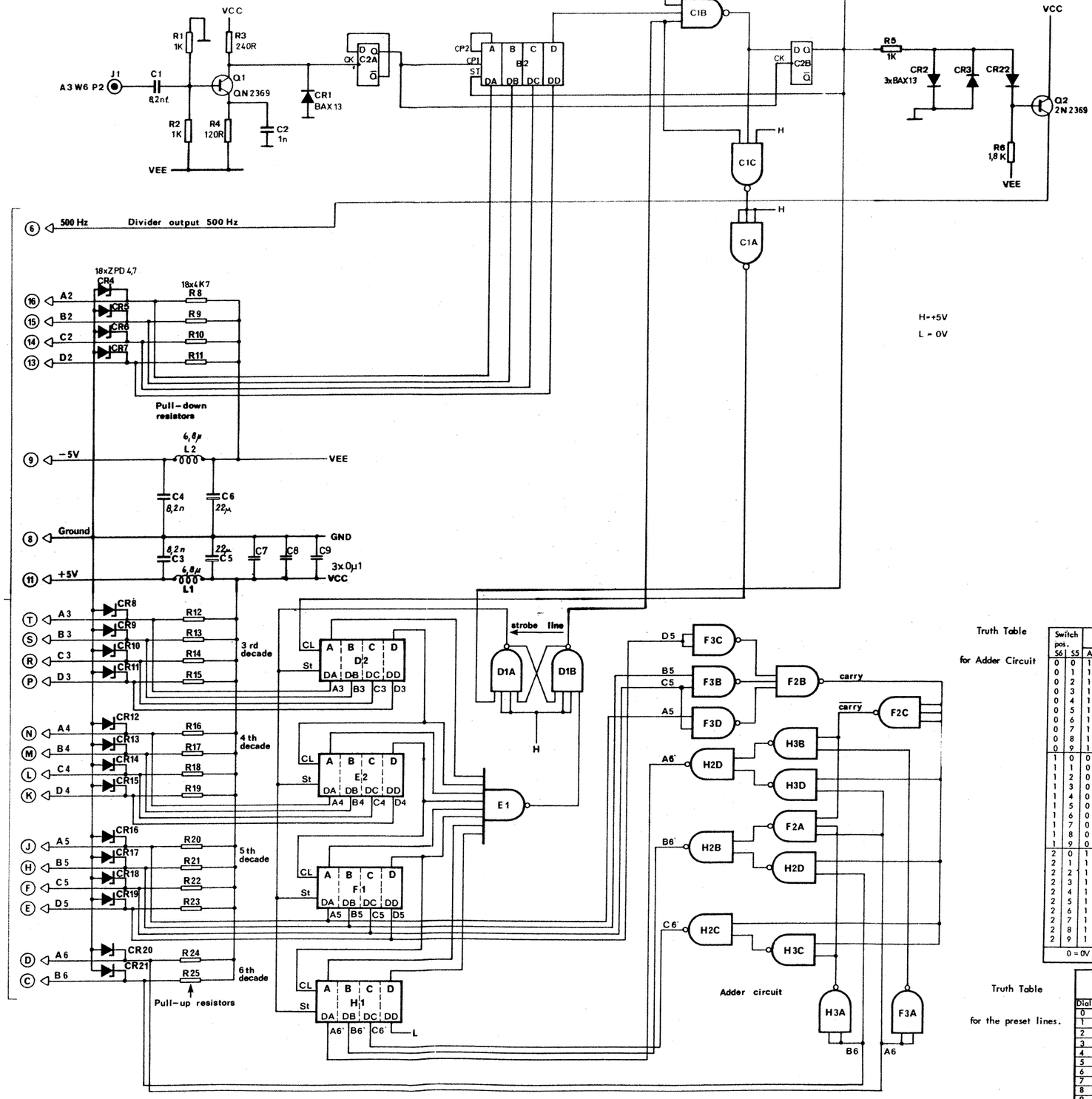
P.C. Card 18813

Card edge

A B C D E F H J K L M N P R S T

P1

(A3J7) ← 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16



Truth Table for Adder Circuit

Switch pos. S6	S5	Input A6	B6	A5	B5	C5	D5	Output A6	B6	C6	Output frequency MHz
0	0	1	0	0	0	1	0	0	1	1	35
0	1	1	0	1	0	1	0	0	1	1	36
0	2	1	0	0	1	0	0	0	1	1	37
0	3	1	0	1	0	0	0	0	1	1	38
0	4	1	0	0	0	0	0	0	1	1	39
0	5	1	0	1	0	0	1	1	0	1	40
0	6	1	0	0	0	0	1	1	0	1	41
0	7	1	0	1	1	1	0	1	0	1	42
0	8	1	0	0	1	1	0	1	0	1	43
0	9	1	0	1	0	1	0	1	0	1	44
1	0	0	0	0	0	1	0	1	0	1	45
1	1	0	0	1	1	0	0	1	0	1	46
1	2	0	0	0	1	0	0	1	0	1	47
1	3	0	0	1	0	0	0	1	0	1	48
1	4	0	0	0	0	0	0	1	0	1	49
1	5	0	0	1	0	0	1	0	0	1	50
1	6	0	0	0	0	0	1	0	0	1	51
1	7	0	0	1	1	1	0	0	0	1	52
1	8	0	0	0	1	1	0	0	0	1	53
1	9	0	0	1	0	1	0	0	0	1	54
2	0	1	1	0	0	1	0	0	0	1	55
2	1	1	1	1	0	0	0	0	0	1	56
2	2	1	1	0	1	0	0	0	0	1	57
2	3	1	1	1	0	0	0	0	0	1	58
2	4	1	1	0	0	0	0	0	0	1	59
2	5	1	1	1	0	0	1	1	1	0	60
2	6	1	1	0	0	0	1	1	1	0	61
2	7	1	1	1	1	0	1	1	1	0	62
2	8	1	1	0	1	1	0	1	1	0	63
2	9	1	1	1	0	1	0	1	1	0	64
		0 = 0V				1 = +5V					

Truth Table for the preset lines.

	1 kHz dec. Sw. S2				10 kHz dec. Sw. S3				100 kHz dec. Sw. S4				1 MHz dec. Sw. S5				10 MHz dec. Sw. S6
Dial	A2	B2	C2	D2	A3	B3	C3	D3	A4	B4	C4	D4	A5	B5	C5	D5	A6	B6	C6
0	1	0	0	1	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
1	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1	0	0	0	1
2	1	1	1	0	1	1	1	0	1	1	1	0	0	1	1	0	1	0	1
3	0	1	1	0	0	1	1	0	0	1	1	0	1	1	1	0	0	1	1
4	1	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	1
5	0	0	1	0	0	0	1	0	0	0	1	0	0	1	0	0	1	0	1
6	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0	1	0	1
7	0	1	0	0	0	1	0	0	0	1	0	0	1	0	0	0	1	1	0
8	1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	1	1	0
9	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	0
	0 = 0V 1 = −5V				0 = 0V 1 = 5V														

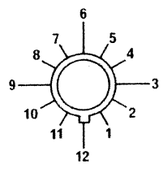
Note 1:
Unless otherwise specified:-
All resistance values are in ohms.
All capacitance values are in microfarads.
All inductance values are in henries.

Note 2:
Partial Reference Designations are shown.
For Complete Designation prefix with Assembly and Subassembly Reference Designations.

Note 3:
Gates, flip-flops, etc. contained in an integrated-circuit package (IC) are identified by ref. designations shown on the individual logic-circuit symbols, e.g.
B3A is gate A contained in ICB3.
The first letter and the following number are also used as coordinates to specify the physical location of the IC on the p.c. card.

35.000-64.999 MHz Variable-Ratio Frequency Divider

Ref. Designation A3A7



Note 1:
Unless otherwise specified:-
All resistance values are in ohms.
All capacitance values are in microfarads.
All inductance values are in henries.

Note 2:
Partial Reference Designations are shown.
For Complete Designation prefix with Assembly and Subassembly Reference Designations, e.g.
R1 of Assembly A4 is A4R1,
R1 of Subassembly A4A1 is A4A1R1,
etc.

J2 → (W5P2)
UG-290 A/U

(A5P1) (J9) (A5P2) (J6)
P4 P1 P2 P3

see Note
A4 A1
P.C. Board 18805

A4A2
P.C. Board 19241/19721
see Note

P.C. Board 19242

P.C. Board 18807

P.C. Board 19121

P.C. Board 18819

P.C. Board 20389

P.C. Board 19429

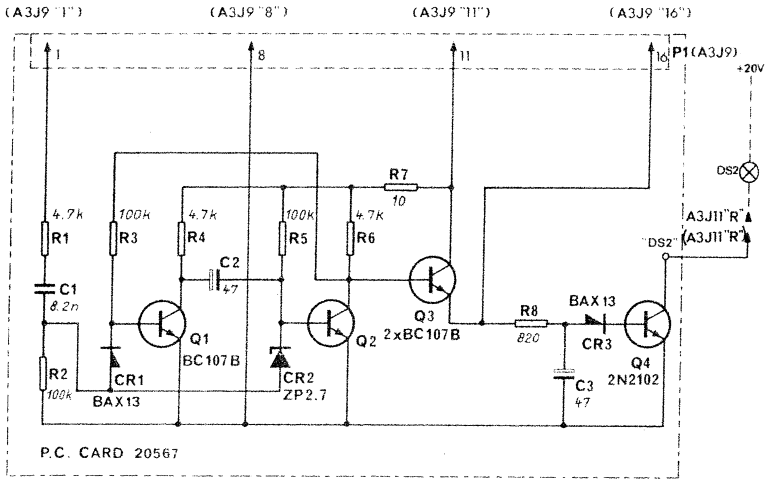
P.C. Board 19432

(P4) ← J1
DB 25P

1 2 - 220V a.c. supply.
3 Relay reduced filament supply.
4 +24V d.c.
5 Pos. "Ia" - mA-meter.
6
7 Pos. "Vg2" - mA-meter.
8 Ground
9 Tune
10 Ground
11 Overload pilot lamp.
12 13 - Overload control sensor.
14 0-1 MHz
15 1-4 MHz
16 1-7 MHz
17 7-30 MHz - Relay control.
18 1-30 MHz
19
20
21
22
23
24
25

Power Amplifier Circuit

Ref. Designations A4, A4A1 and A4A2



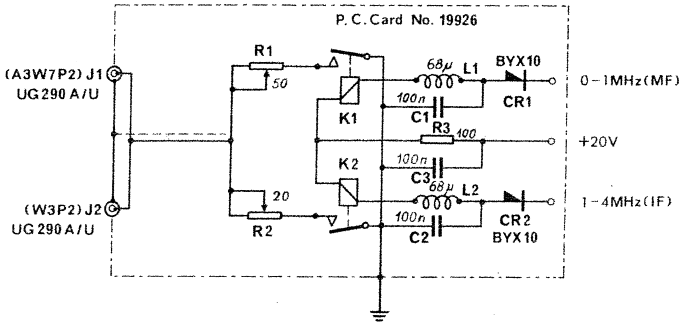
Note 1:
Unless otherwise specified:-
All resistance values are in ohms.
All capacitance values are in microfarads.
All inductance values are in henries.

Note 2:
Partial Reference Designations are shown.
For Complete Designation prefix with Assembly and Subassembly Reference Designations.

Output Gate-Off Circuit

S 1250 Diagr. No. 4086/7.71

Ref. Designation A3A8

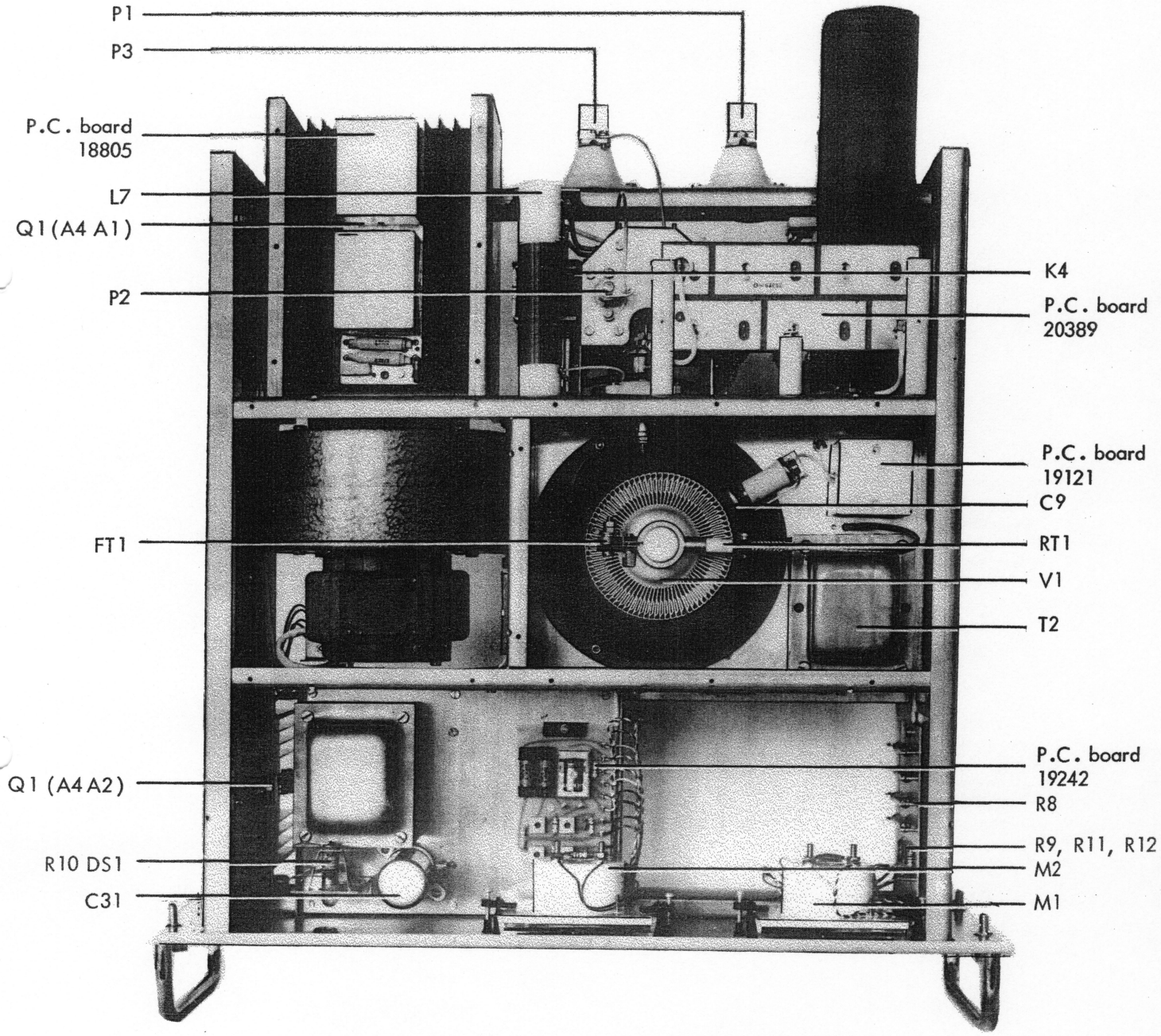


Note 1:
Unless otherwise specified:-
All resistance values are in ohms.
All capacitance values are in microfarads.
All inductance values are in henries.

Note 2:
Partial Reference Designations are shown.
For Complete Designation prefix with Assembly and Subassembly Reference Designations.

1.5-MHz Signal-Level Control Circuit

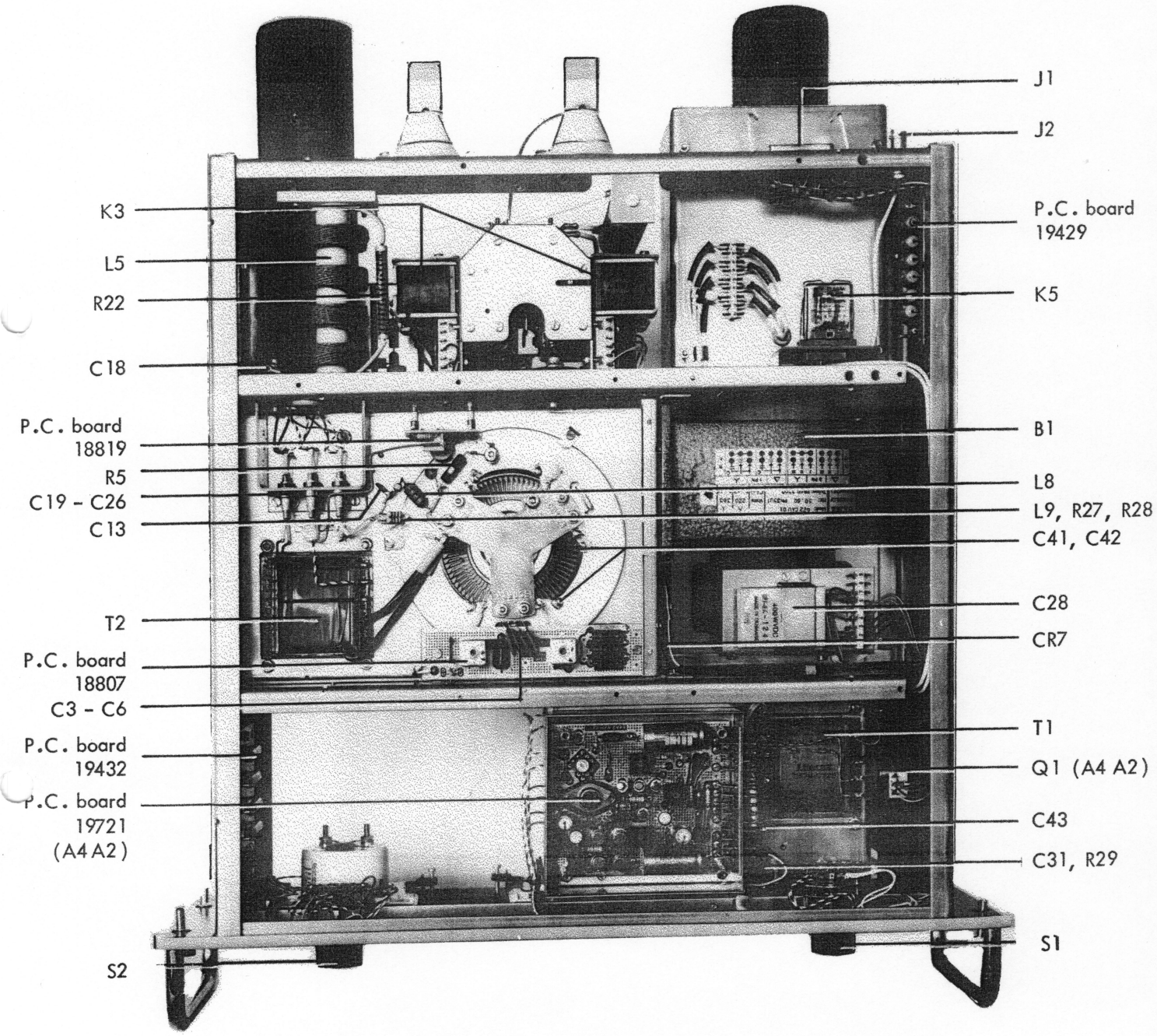
Ref. Designation A3A9



Power Amplifier Circuit

Ref. Designations A4, A4A1 and A4A2

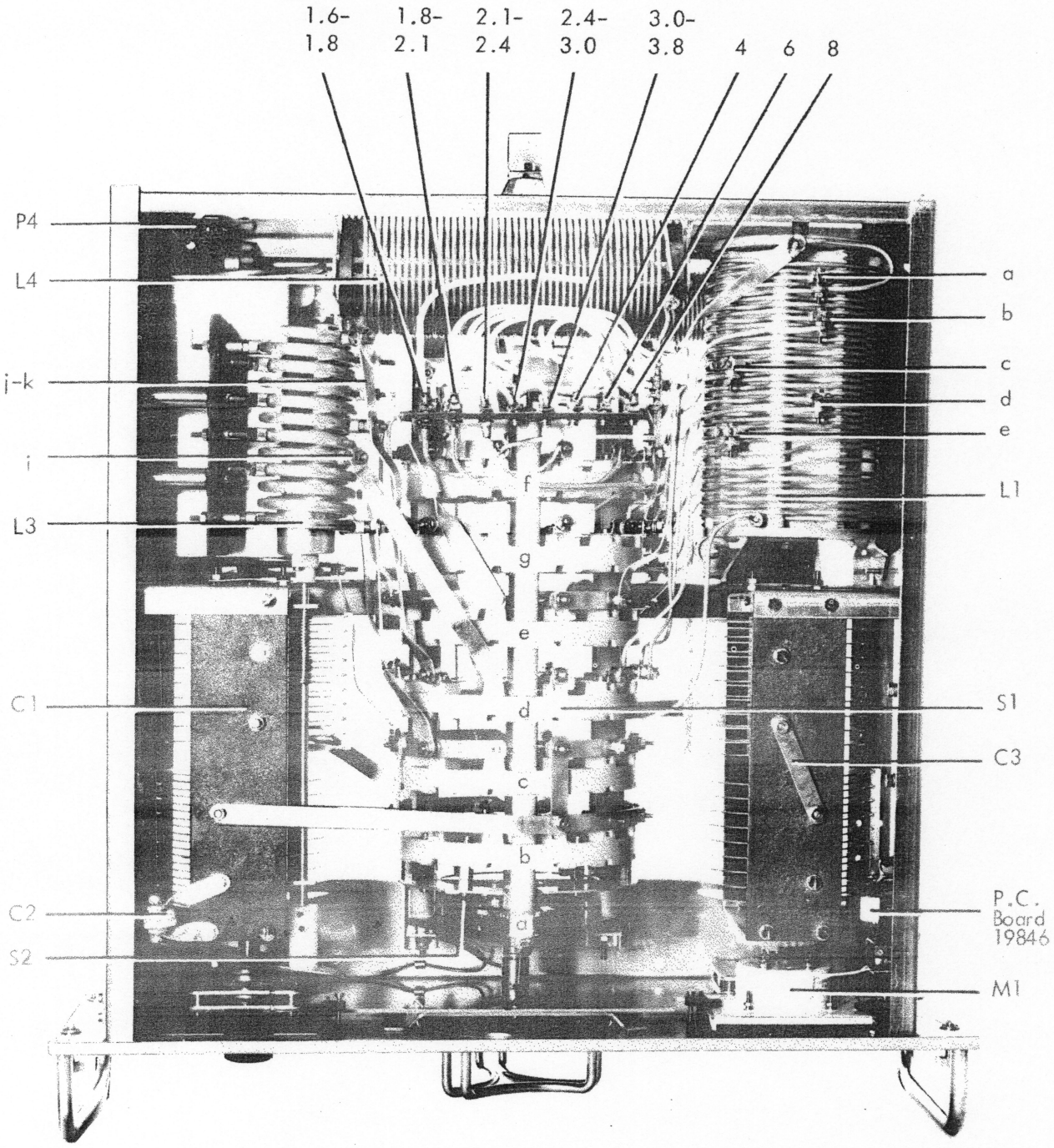
Top View



Power Amplifier Circuit

Bottom View

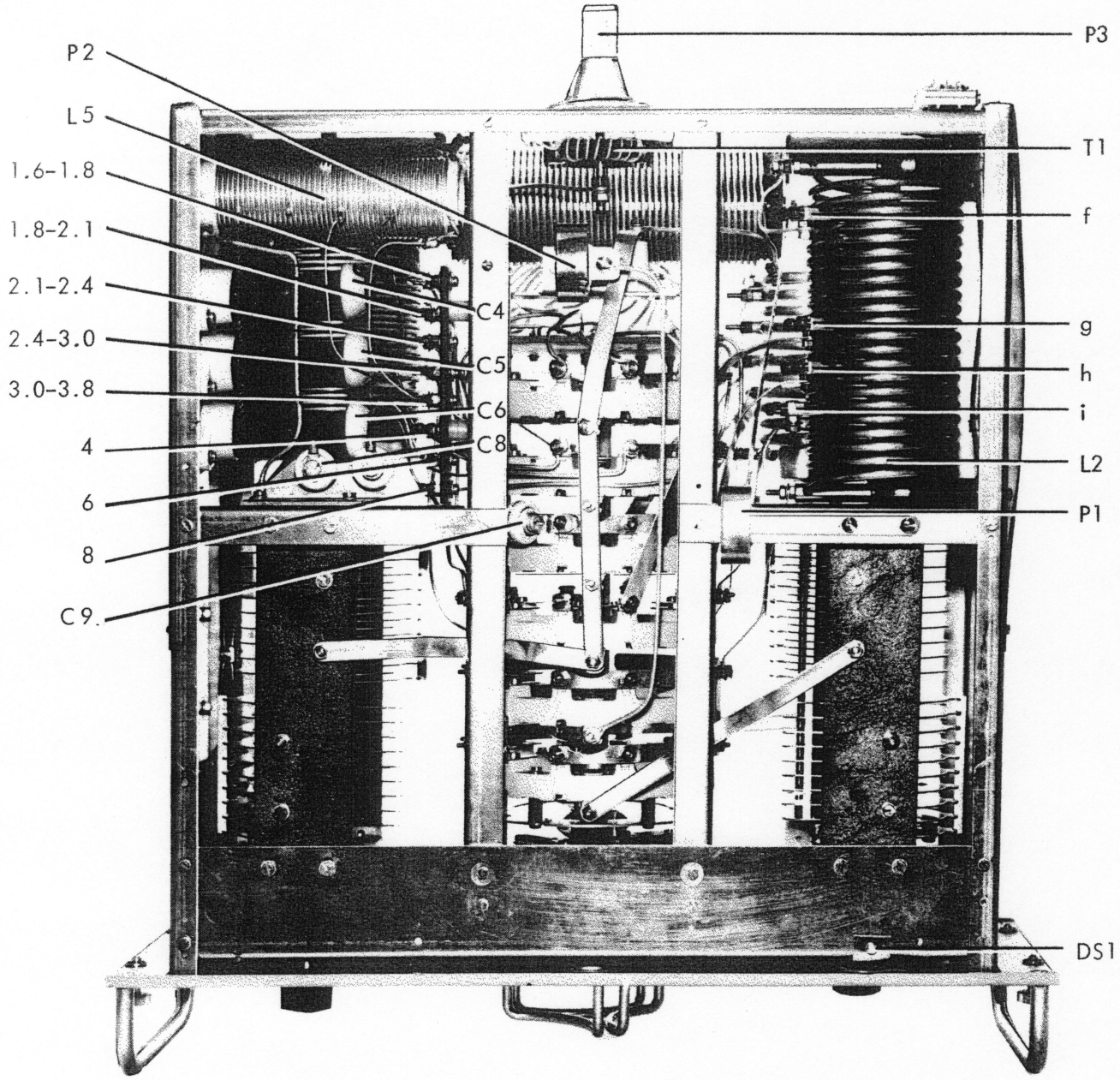
Ref. Designations A4, A4A1 and A4A2



Intermediate-Frequency and High-Frequency
Antenna Matching Network

Top View

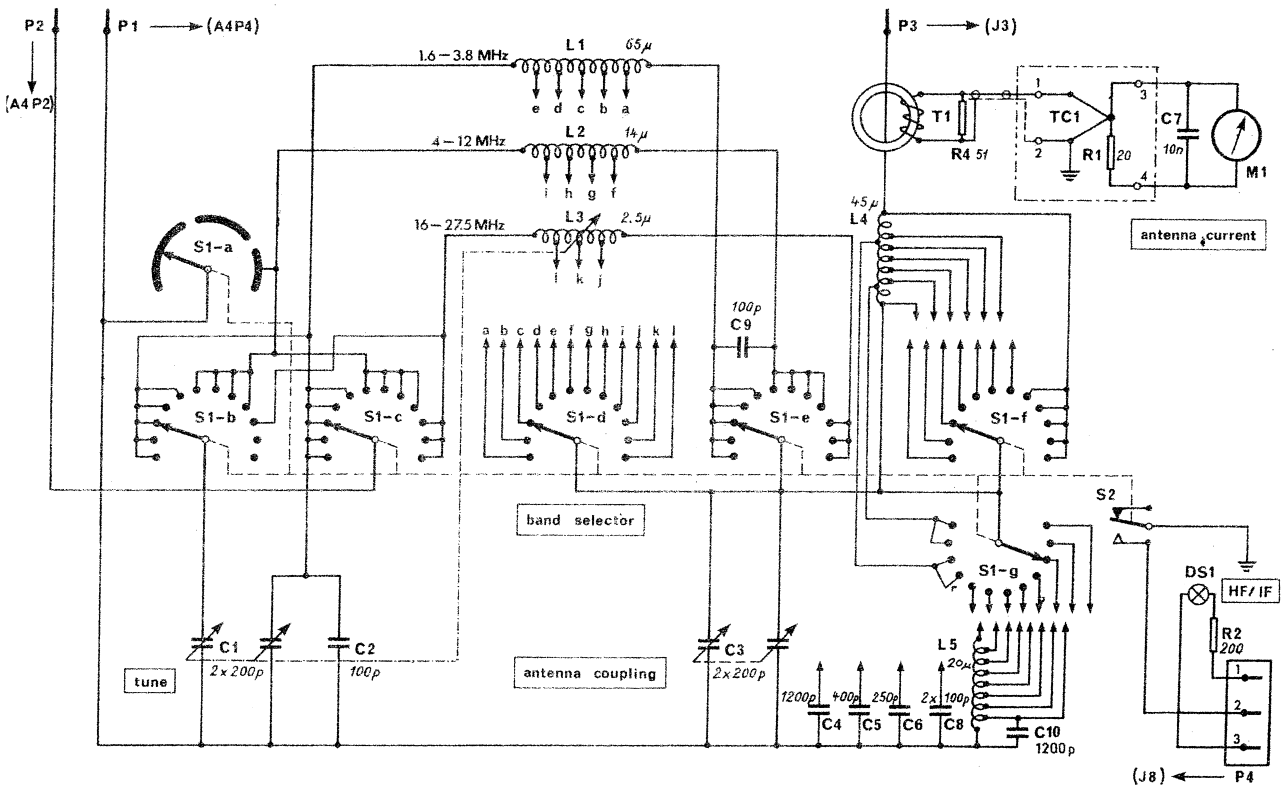
Ref. Designation A5



Intermediate-Frequency and High-Frequency
Antenna Matching Network

Bottom View

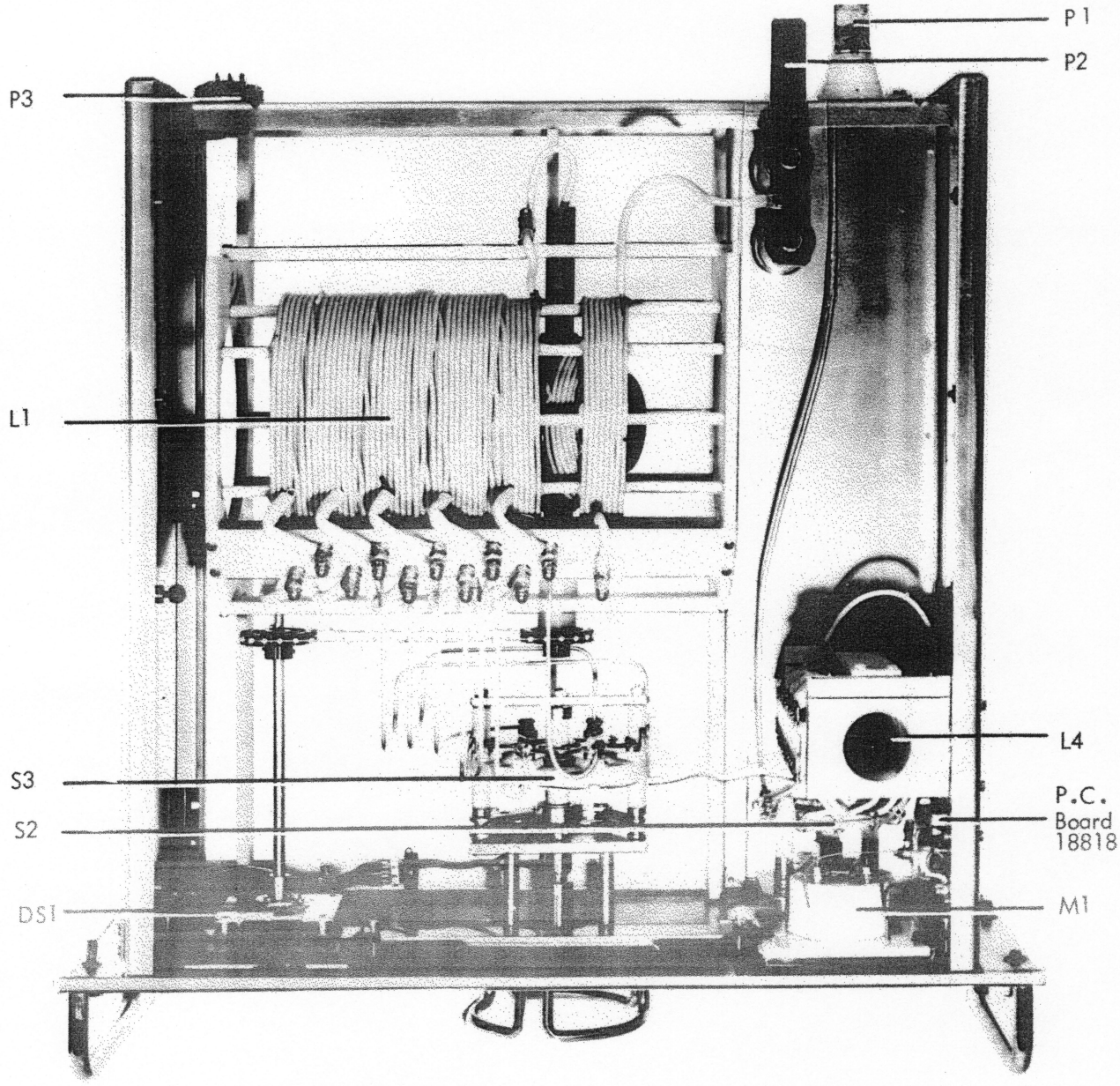
Ref. Designation A5



Note 1:
Unless otherwise specified:-
All resistance values are in ohms.
All capacitance values are in microfarads.
All inductance values are in henries.

Note 2:
Partial Reference Designations are shown.
For Complete Designation prefix with Assembly and Subassembly Reference Designations.

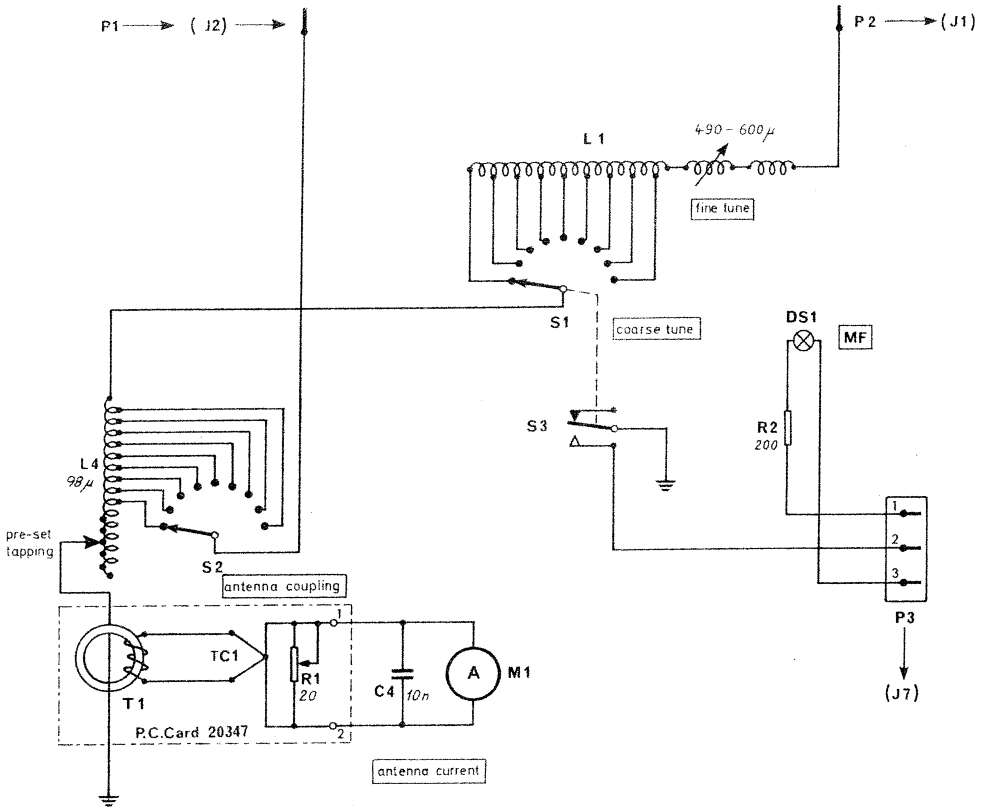
Intermediate-Frequency and High-Frequency Antenna Matching Network



Medium-Frequency Antenna Matching Network

Top View

Ref. Designation A6



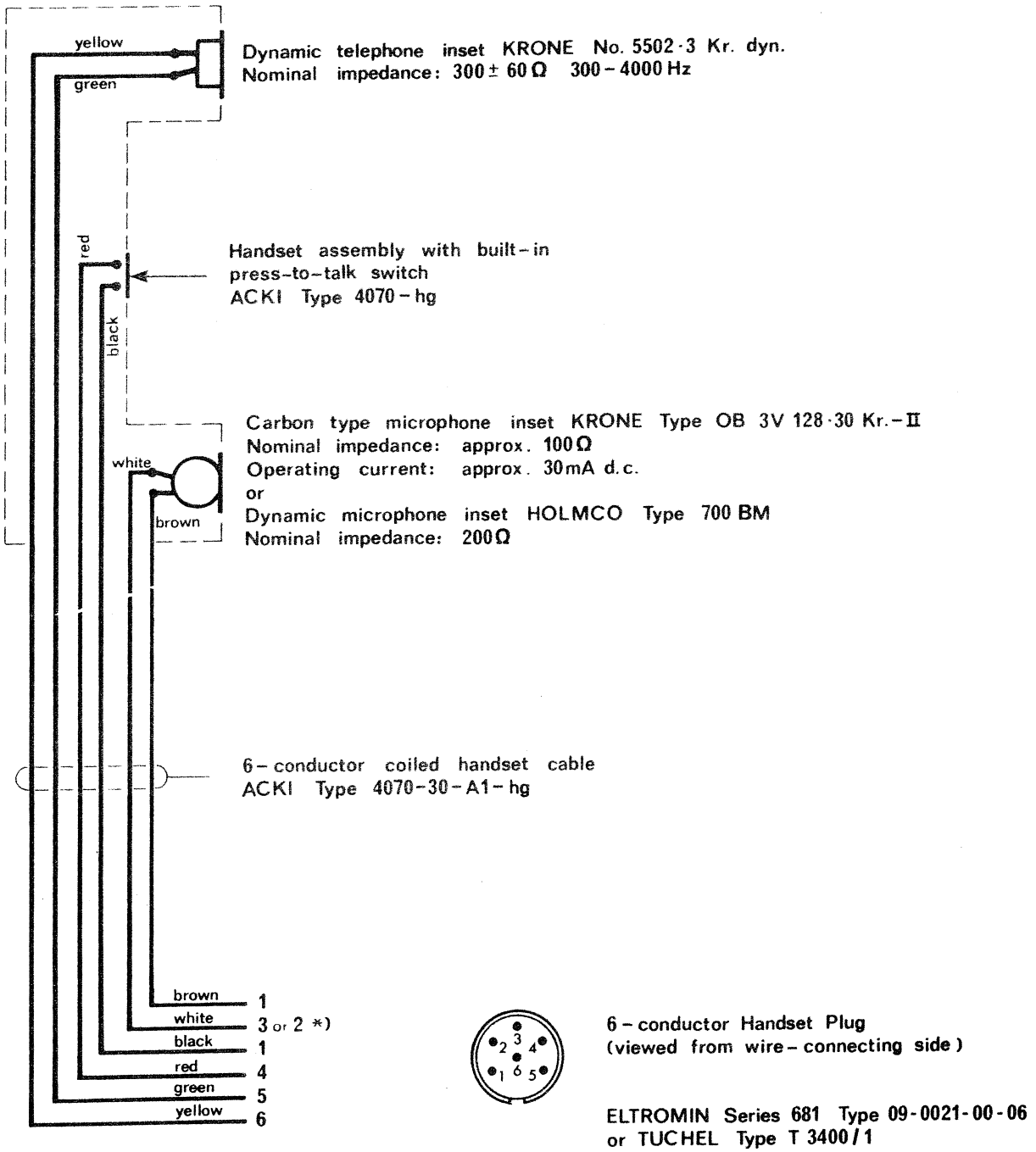
Note 1:
Unless otherwise specified:-
All resistance values are in ohms.
All capacitance values are in microfarads.
All inductance values are in henries.

Note 2:
Partial Reference Designations are shown.
For Complete Designation prefix with Assembly and Subassembly Reference Designations.

Medium-Frequency Antenna Matching Network

S 1250 Diagr. No.4393/4.76

Ref. Designation A6

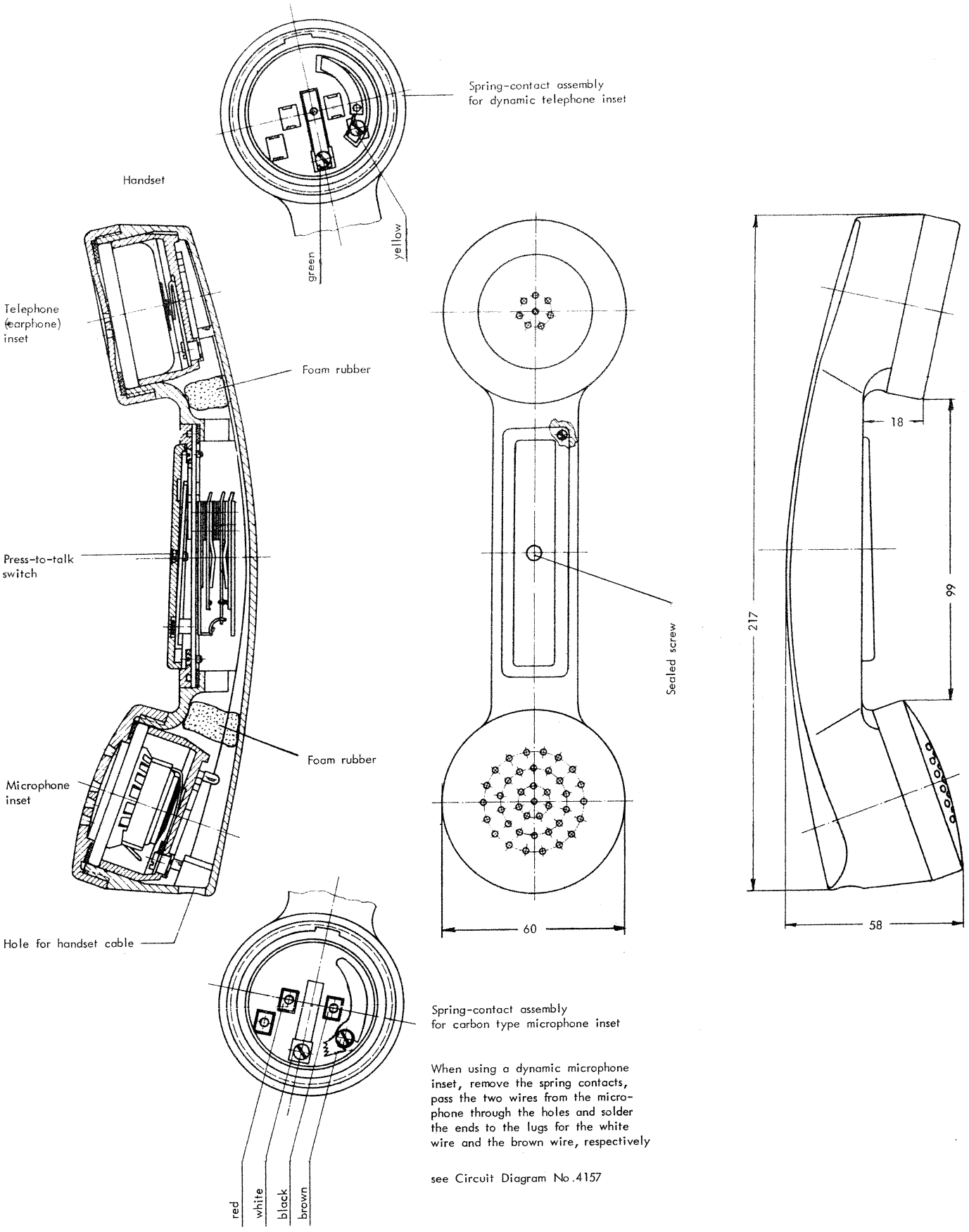


*) For handsets with carbon type microphone connect the white wire to plug contact No. 3
For handsets with dynamic microphone connect the white wire to plug contact No. 2

Handset Type HS 1250

Circuit Diagram

Diagr. No. 4157/3-71



When using a dynamic microphone inset, remove the spring contacts, pass the two wires from the microphone through the holes and solder the ends to the lugs for the white wire and the brown wire, respectively

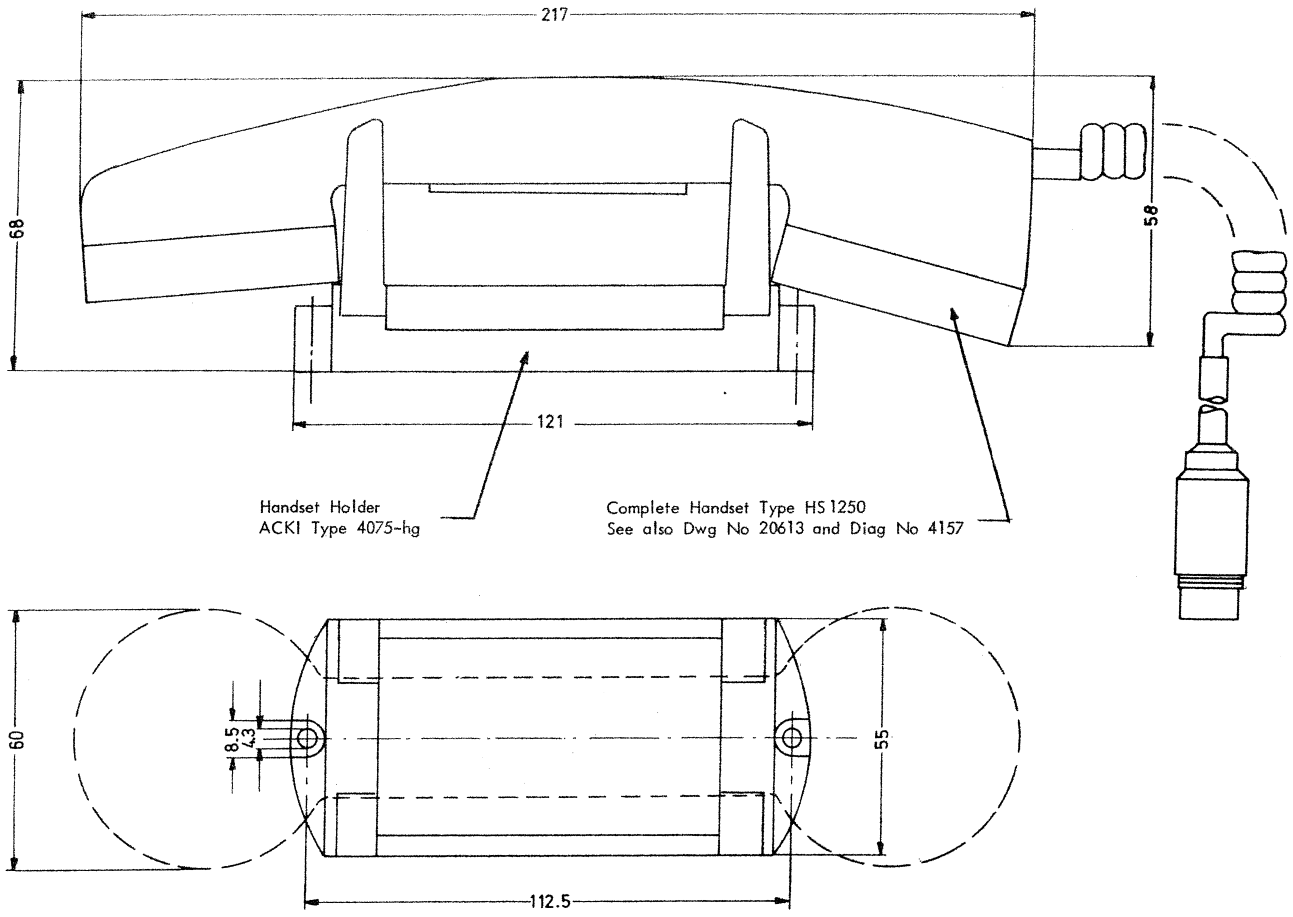
see Circuit Diagram No.4157

All dimensions are in mm (NTS)

Handset Type HS 1250

Outline Dimensions

Drwg. No. 20613/3-71

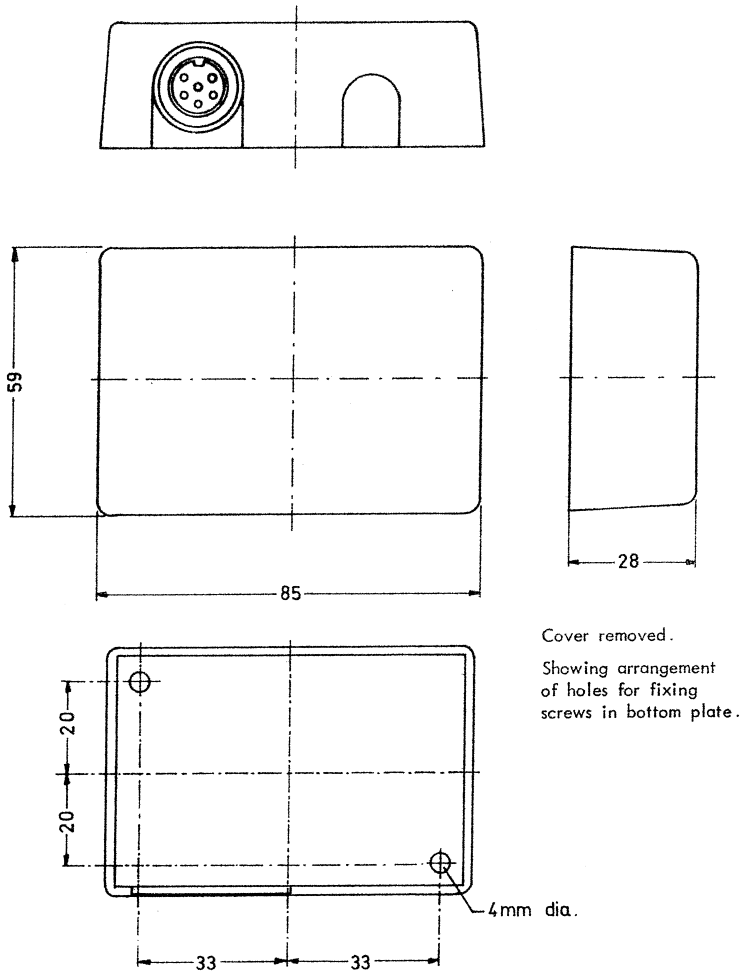


All dimensions are in mm (NTS)

Handset Type HS 1250 and Handset Holder

Outline and Mounting Dimensions

Dwg No 20806/11-71



Cover removed.

Showing arrangement of holes for fixing screws in bottom plate.

All dimensions are in mm (NTS)

When the main receiver associated with the main transmitter is mounted together with the auto alarm, reserve transmitter, reserve receiver, etc. in a common rack, the handset holder and the handset socket are located on the common rack. For installations where other arrangements for the receivers are used, the outlet box Type 20653 shown above can be supplied on special order.

Outlet Box Type 20653

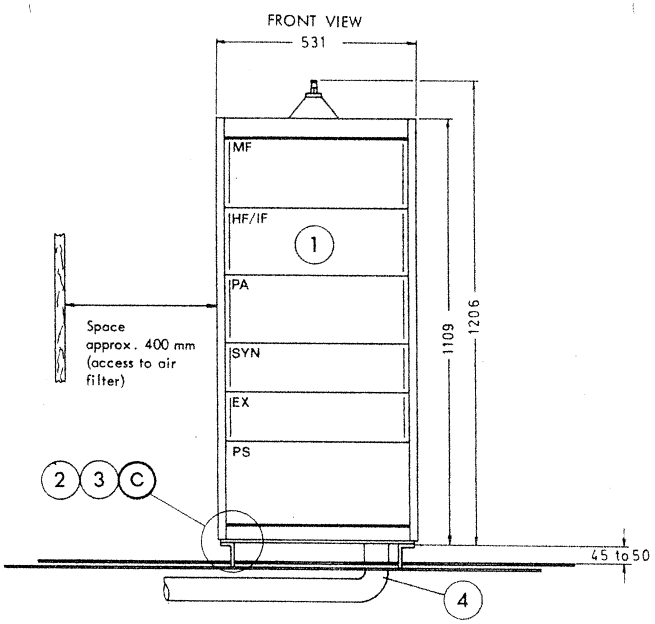
Outline and Mounting Dimensions

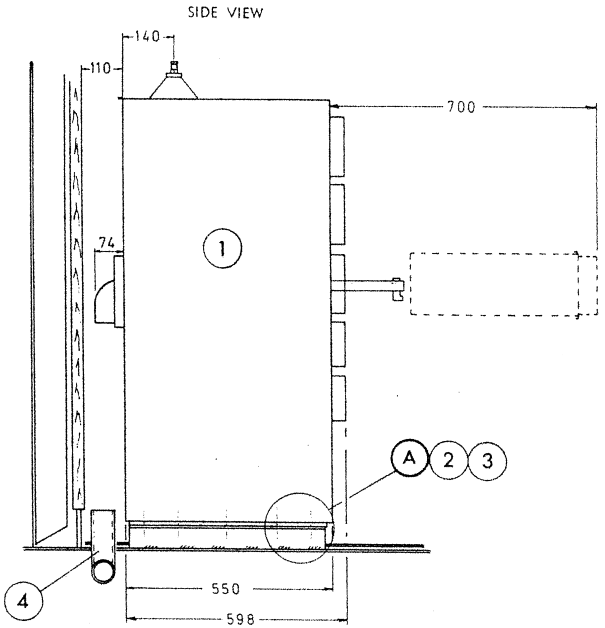
Dwg No 20805/11-71

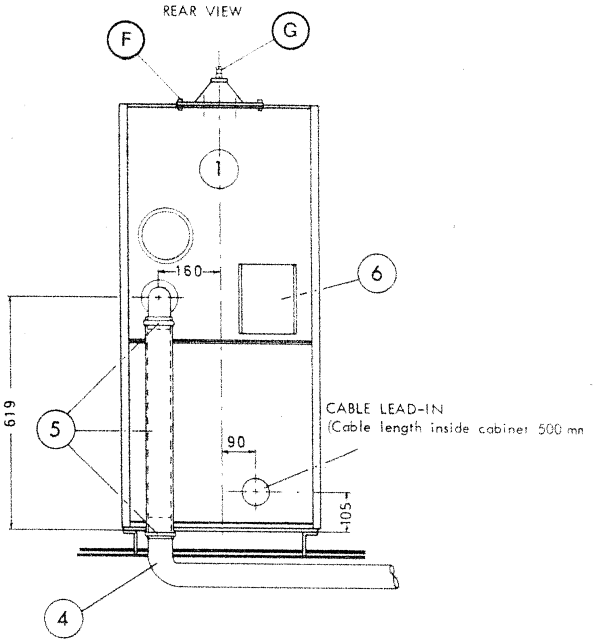
S 1250 Drwg. No. 20510/3-71

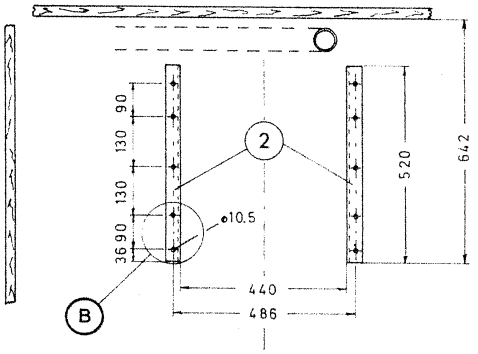
Main Radio Telegraph and Telephone Transmitter

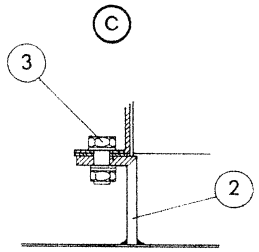
Outline Dimensions and Method of Mounting

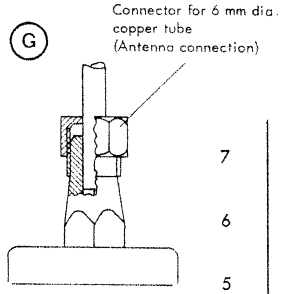


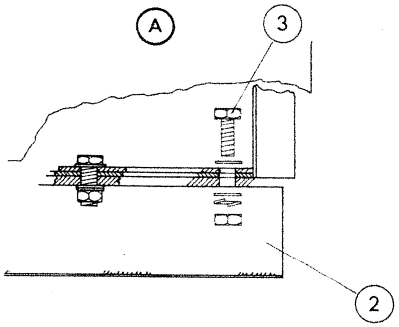


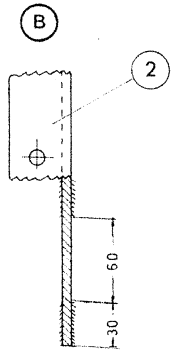


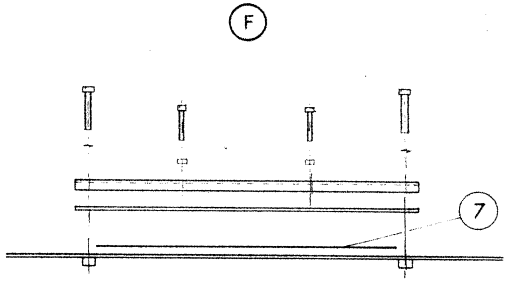










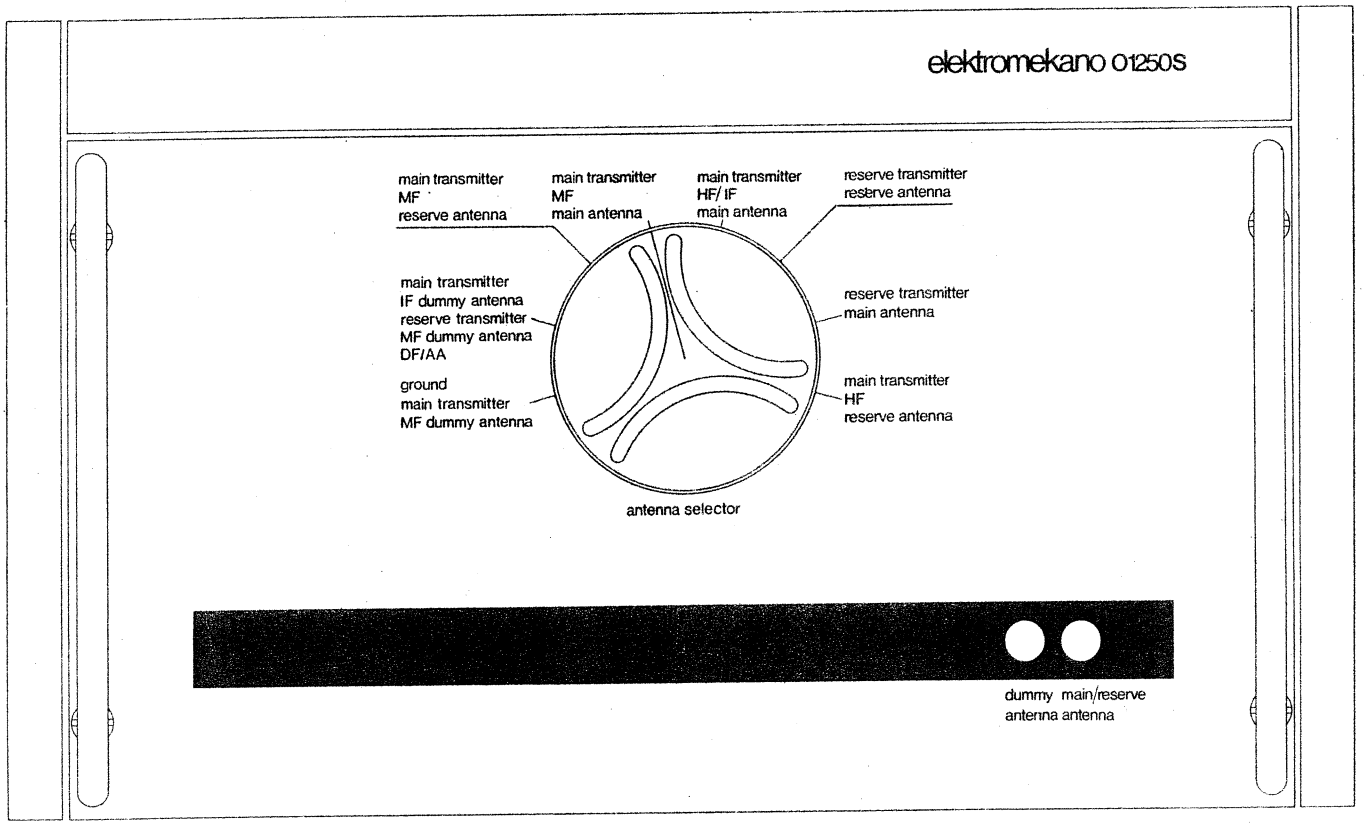


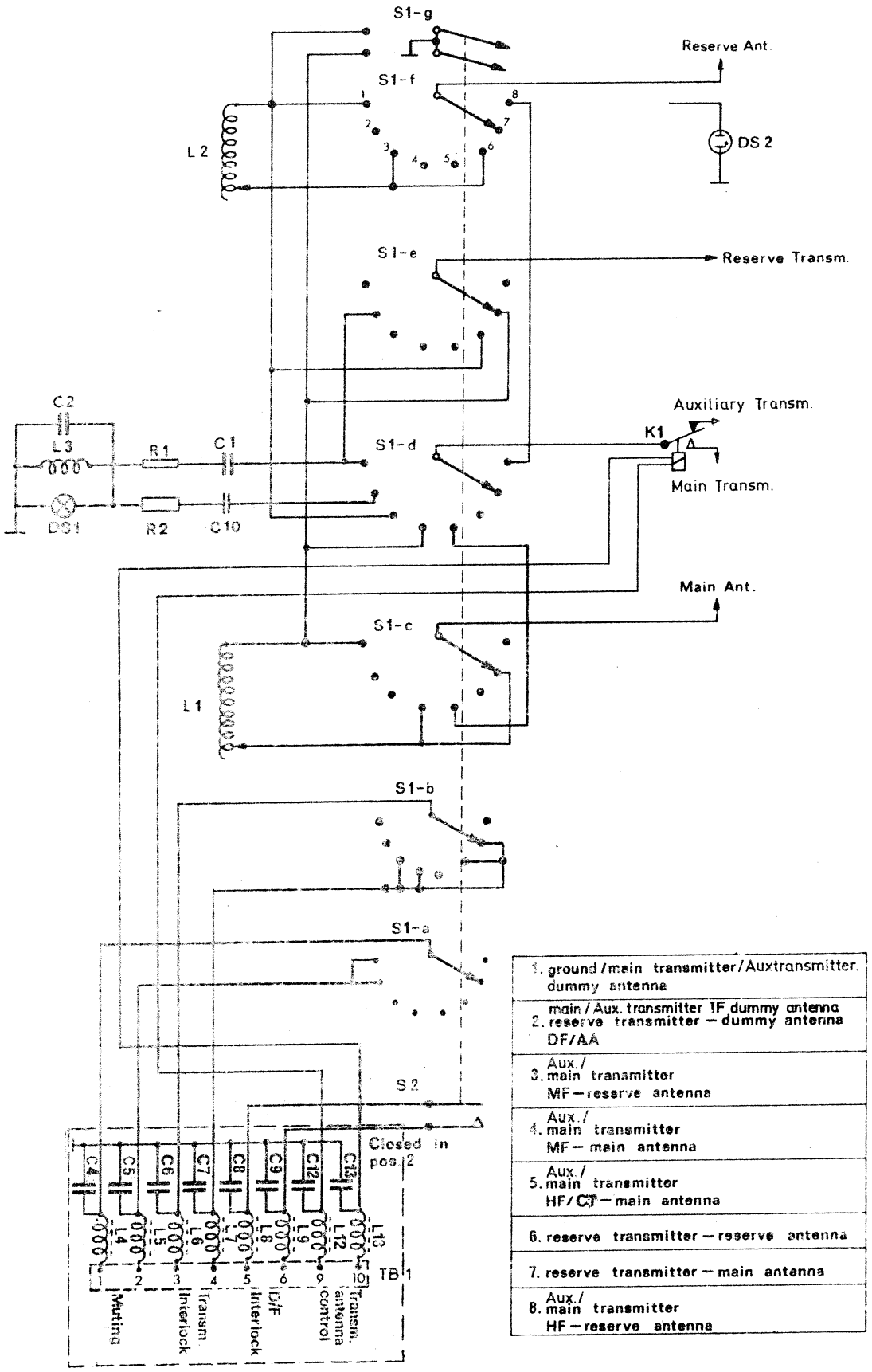
All dimensions are in mm (NTS)

POS. NO.	DESCRIPTION	SEE ALSO DRWG. NO.	SUPPLY
7	COPPER STRIP 200 x 0.4 mm (Installation material)	20545	Manufacturer
6	AIR INTAKE FILTER	20546	Manufacturer
5	FLEXIBLE AIR TUBE with CLAMPS	20546	Manufacturer
4	FITTINGS for FLEXIBLE AIR TUBE (Outside dia. 63 mm)	20546	Shipyard
3	10 FIXING BOLTS (STEEL) 8 x 30 mm with WASHER, SPRING WASHER and LOCKNUTS		Manufacturer
2	2 ANGLE IRONS 60 x 40 x 8 mm (To be placed as shown on this drawing. Correct for camber and sheer)		Shipyard
1	MAIN TRANSMITTER S 1250 (Weight approx. 165 kg)		Manufacturer

instruction manual

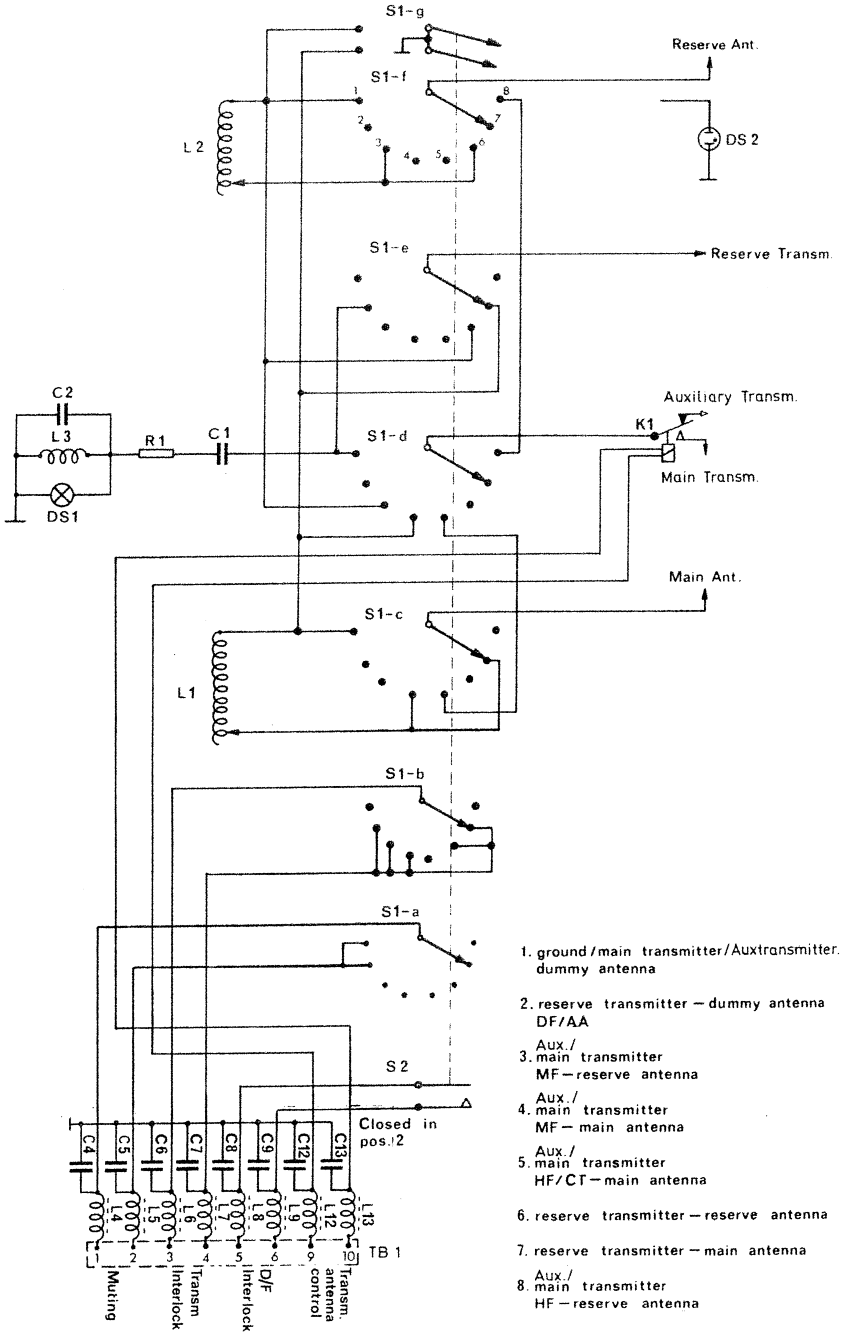
ANTENNA SELECTOR SWITCH



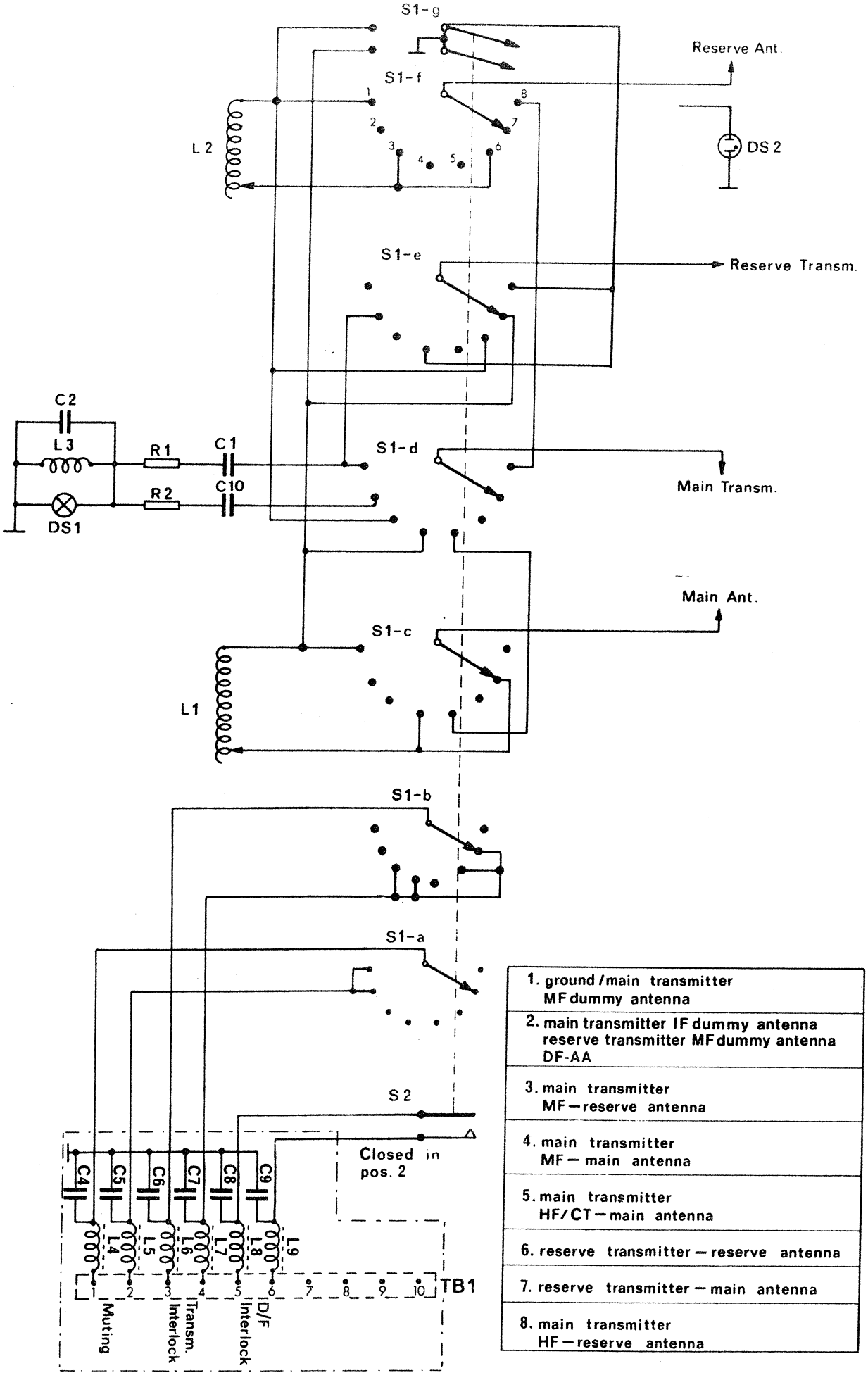


O 1250 KS Diag. No. 4240 / 09-80

Antenna Selector Switch
(Complies with SOLAS 1974)

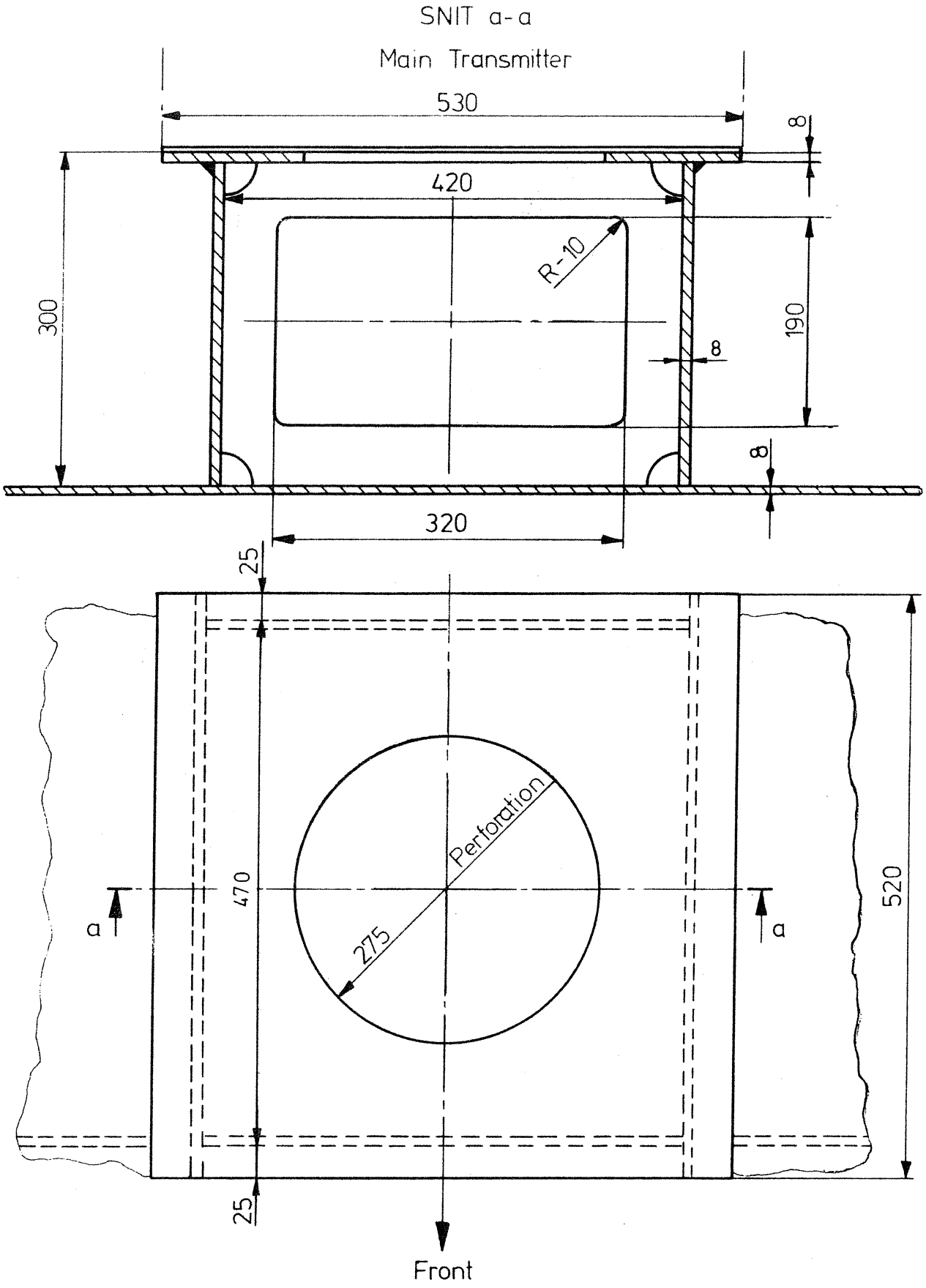


Antenna Selector Switch



1. ground / main transmitter MF dummy antenna
2. main transmitter IF dummy antenna reserve transmitter MF dummy antenna DF-AA
3. main transmitter MF – reserve antenna
4. main transmitter MF – main antenna
5. main transmitter HF/CT – main antenna
6. reserve transmitter – reserve antenna
7. reserve transmitter – main antenna
8. main transmitter HF – reserve antenna

Antenna Selector Switch
(Complies with SOLAS 1974)



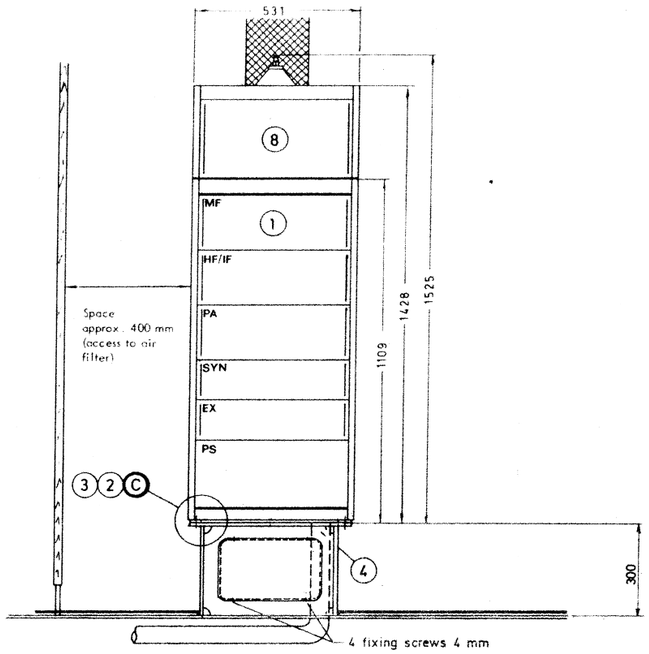
All dimensions are in mm (NTS)

Foundation for Main Transmitter

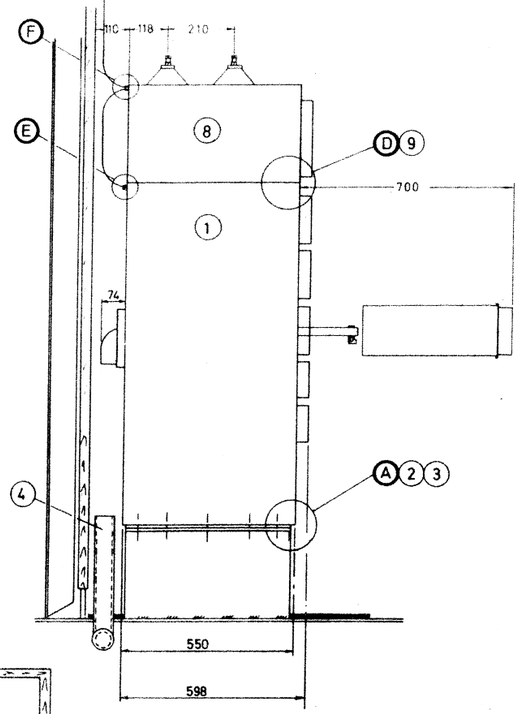
Dwg.No. SX 1498 / 1976-12

Type S 1250

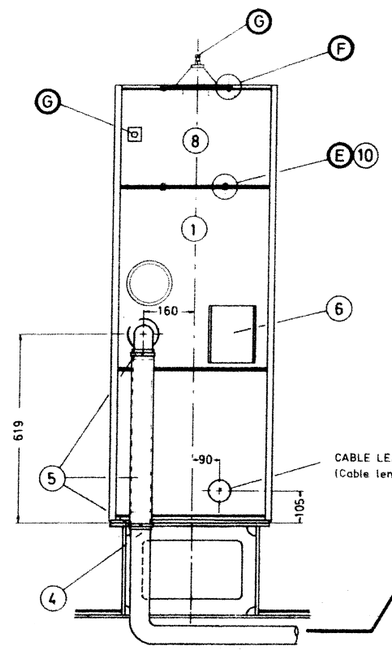
FRONT VIEW



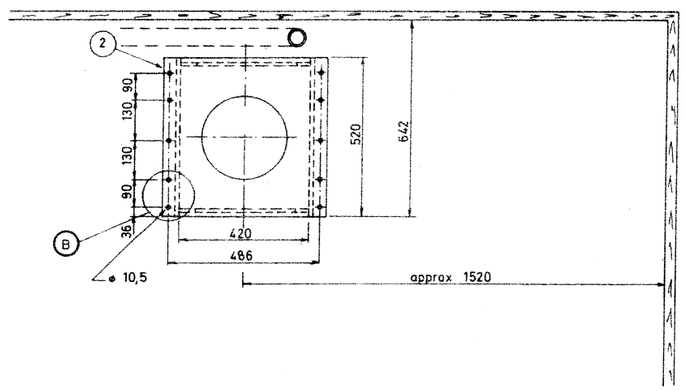
SIDE VIEW

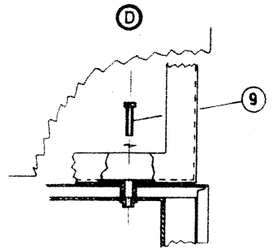


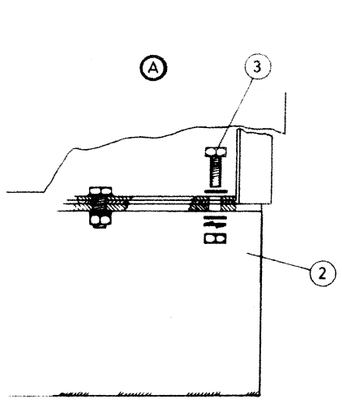
REAR VIEW

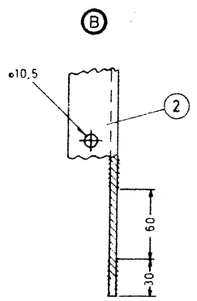


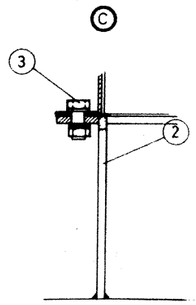
NOT TO THE OPEN AIR BUT TO CORRIDOR OR OTHER WELL-VENTILATED ROOM (MAX. LENGTH 2.5M)
1280 kcal/hour
54 m^3/hour

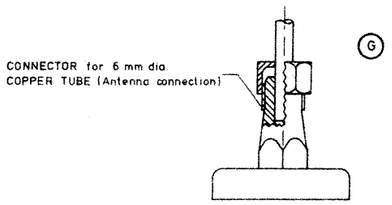


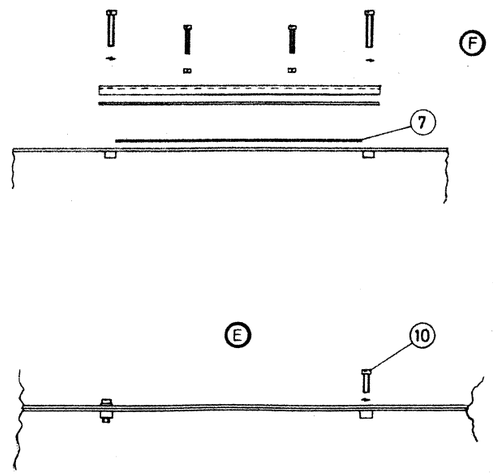












POS. NO.	DESCRIPTION	SEE ALSO DRWG. NO.	SUPPLY
10	2 FIXING SCREWS (STEEL) 5 x 15 mm with WASHER and SPRING WASHER		Manufacturer
9	4 FIXING SCREWS (STEEL) 6 x 30 mm with WASHER and SPRING WASHER		Manufacturer
8	ANTENNA SELECTOR SWITCH O 1250 (Weight approx. 25 kg)		Manufacturer
7	COPPER STRIP 200 x 0.4 mm	20545	Manufacturer
6	AIR INTAKE FILTER	20546	Manufacturer
5	FLEXIBLE AIR TUBE with CLAMPS	20546	Manufacturer
4	FITTINGS for FLEXIBLE AIR TUBE (Outside dia. 63 mm)	20546	Shipyard
3	10 FIXING BOLTS (STEEL) 8 x 30 mm with WASHER, SPRING WASHER and LOCKNUTS		Manufacturer
2	FOUNDATION (To be placed as shown on this drawing. Correct for camber and sheer)	SX 1498/4	Shipyard
1	MAIN TRANSMITTER S 1250 (Weight approx. 165 kg)		Manufacturer

ALL DIMENSIONS IN MILLIMETERS

Main Radio Telegraph and Telephone Transmitter and Antenna Selector Switch

Outline Dimensions and Method of Mounting

S 1250 / O 1250 Drwg. No. 20290/1/ 1980-11